

GA-AX370-GAMING K7

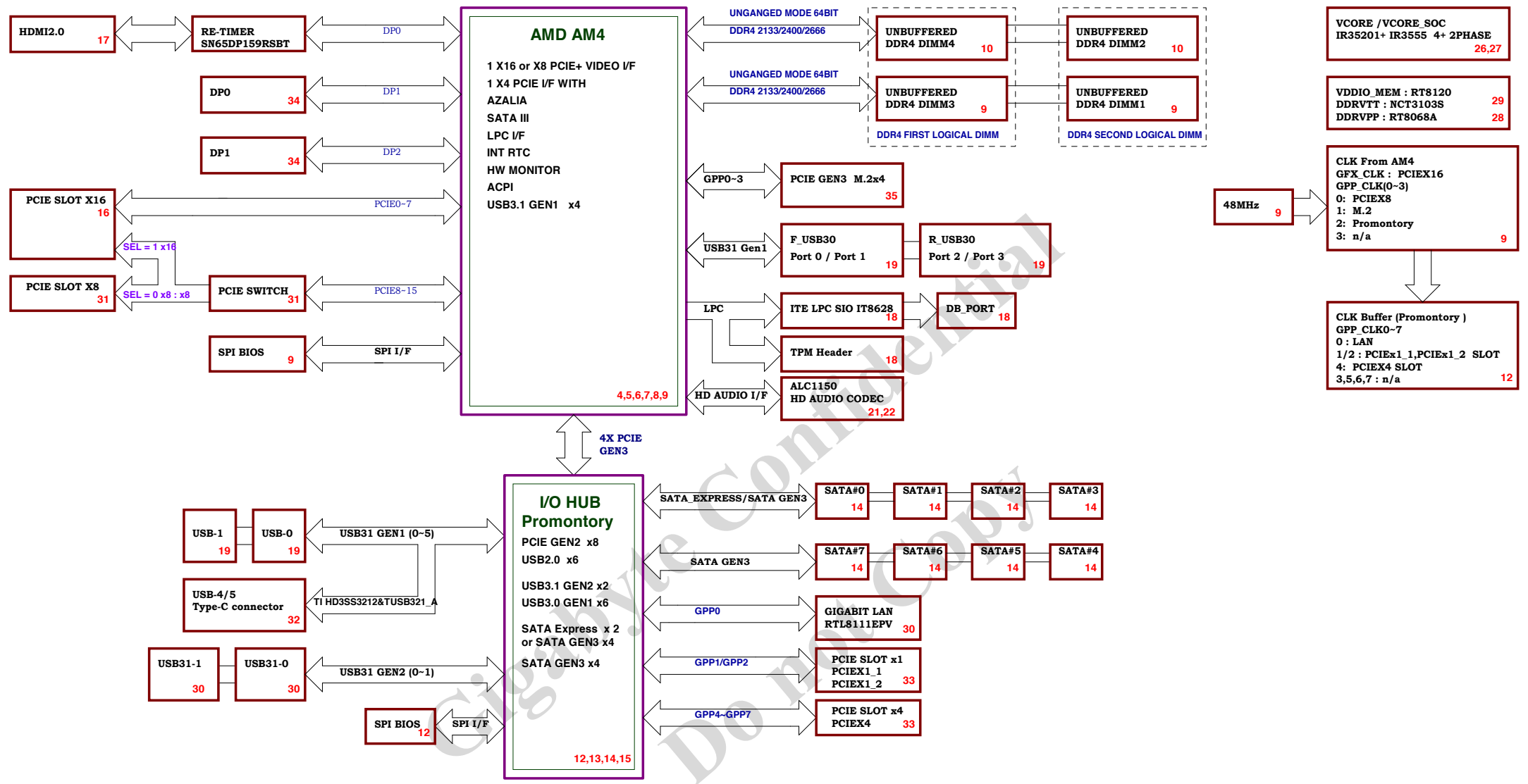
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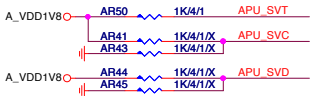
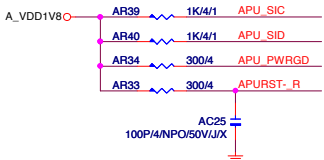
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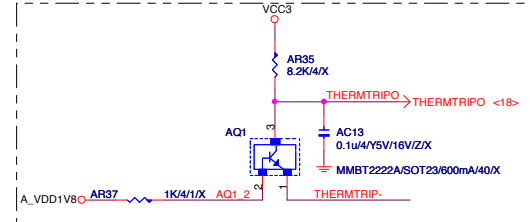
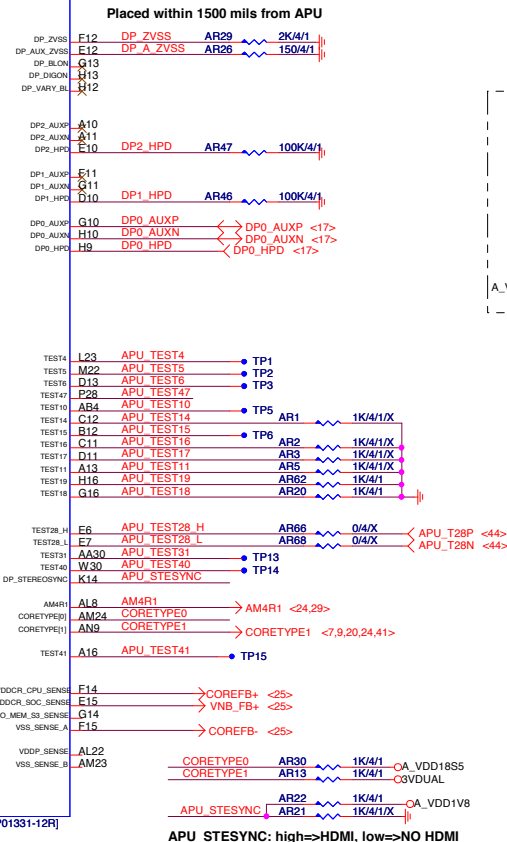
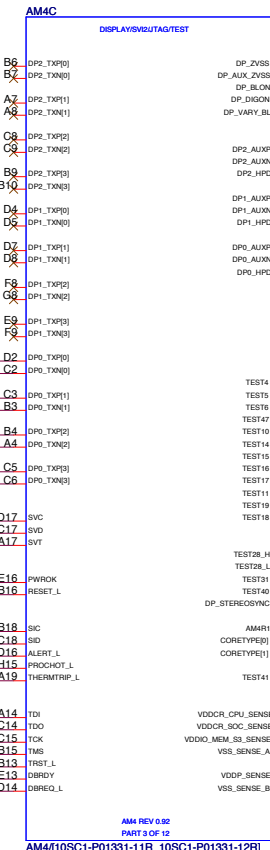
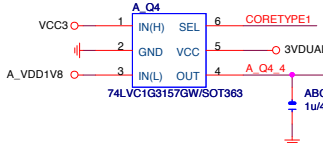
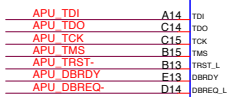
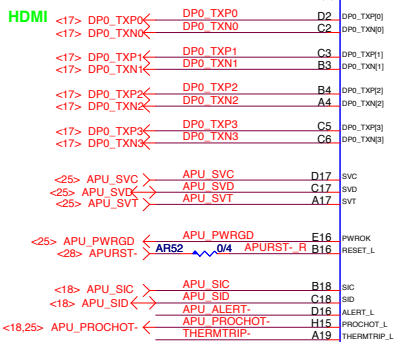
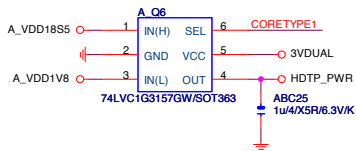
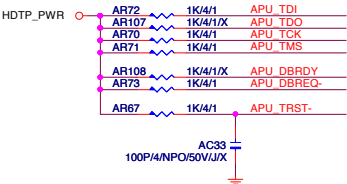
	S		4		3		2		1				
Model Name:GA-AX370-GAMING K7													
Component value change history				Version: 1.0		Circuit or PCB layout change for next version							
				P-Code: U98126-0									
Date	Change Item		Reason										
2016.08.08	01 New BOM Release.	PCB: 0.1	1. OR169 NA										
2017.02.06	1.0A P-BOM Release.	PCB: 10	1. Modify AX370-GAMING 5 10T4 9FGL1214AKLFT 2. LED_REAR 上件 3.R_MOS :12SP2-S08025-F1R T_MOS :12SP2-S09425-R1R PT_MOS : 12SP2-S06912-21R/22R/23R AUDIO_COVER : 12KRC-0A0001-41R REAR_HS : 12KRC-0H0007-51R 4. IR VIN cap 上件 (all 0.1u)										
2017.02.07	1.0B F-BOM Release.	PCB: 10	1. KNOLL NA 2. DAJP NA 3. SLOT CHANGE TO 鍍黑鍍金屬slot										
2017.02.14	1.0C F-BOM Release.	PCB: 10	1. Update new value for DAC power (pull to 3VDual) DCCA_R15 / DACA_R15 NA DCCA_R16 / DACA_R16 上件										

[illegible]





SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



APU_STESYNC: high=>HDMI, low=>NO HDMI

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

GIGABYTE™

Title

CPU CONTROL

Size

Customer

Document Number

GA-AX370-GAMING K7

Rev

1.0

Date:

Tuesday, February 14, 2017

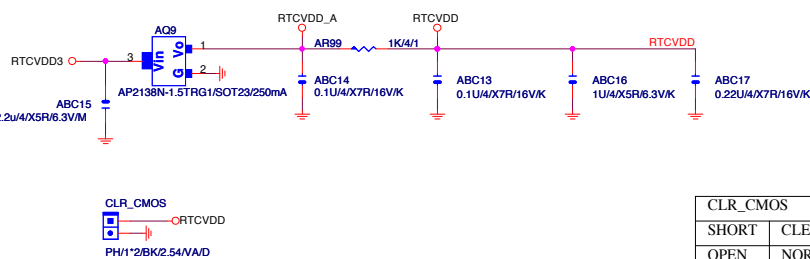
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of

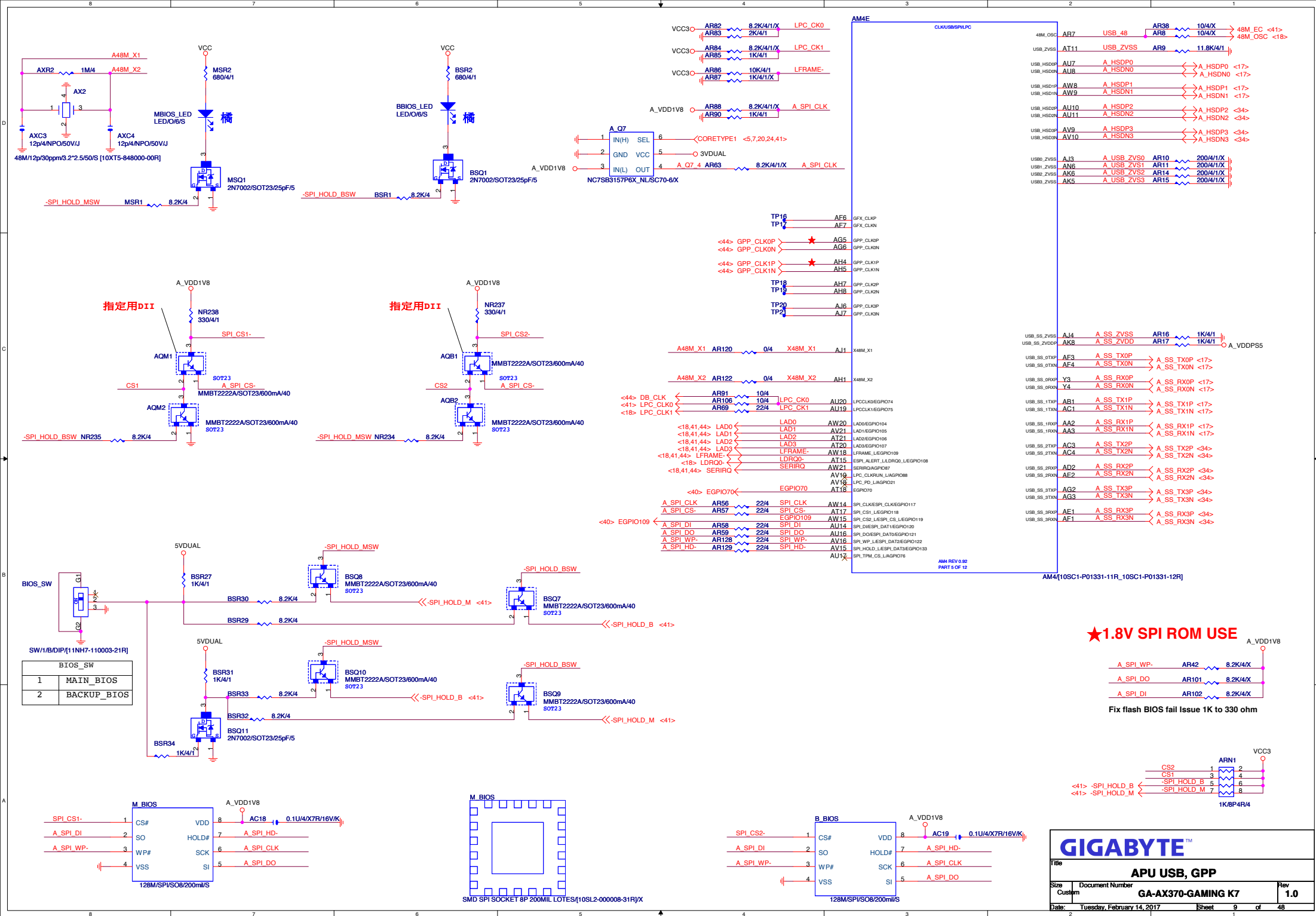
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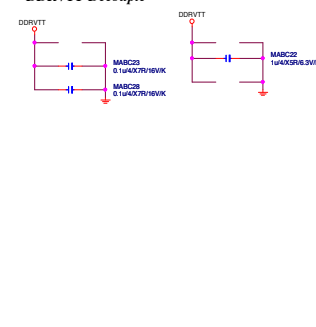
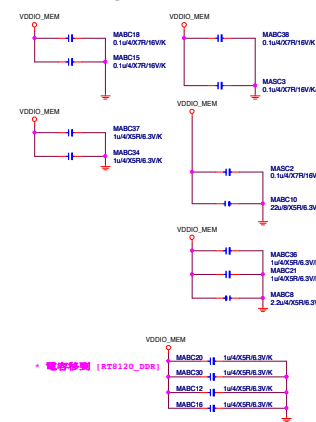
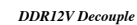
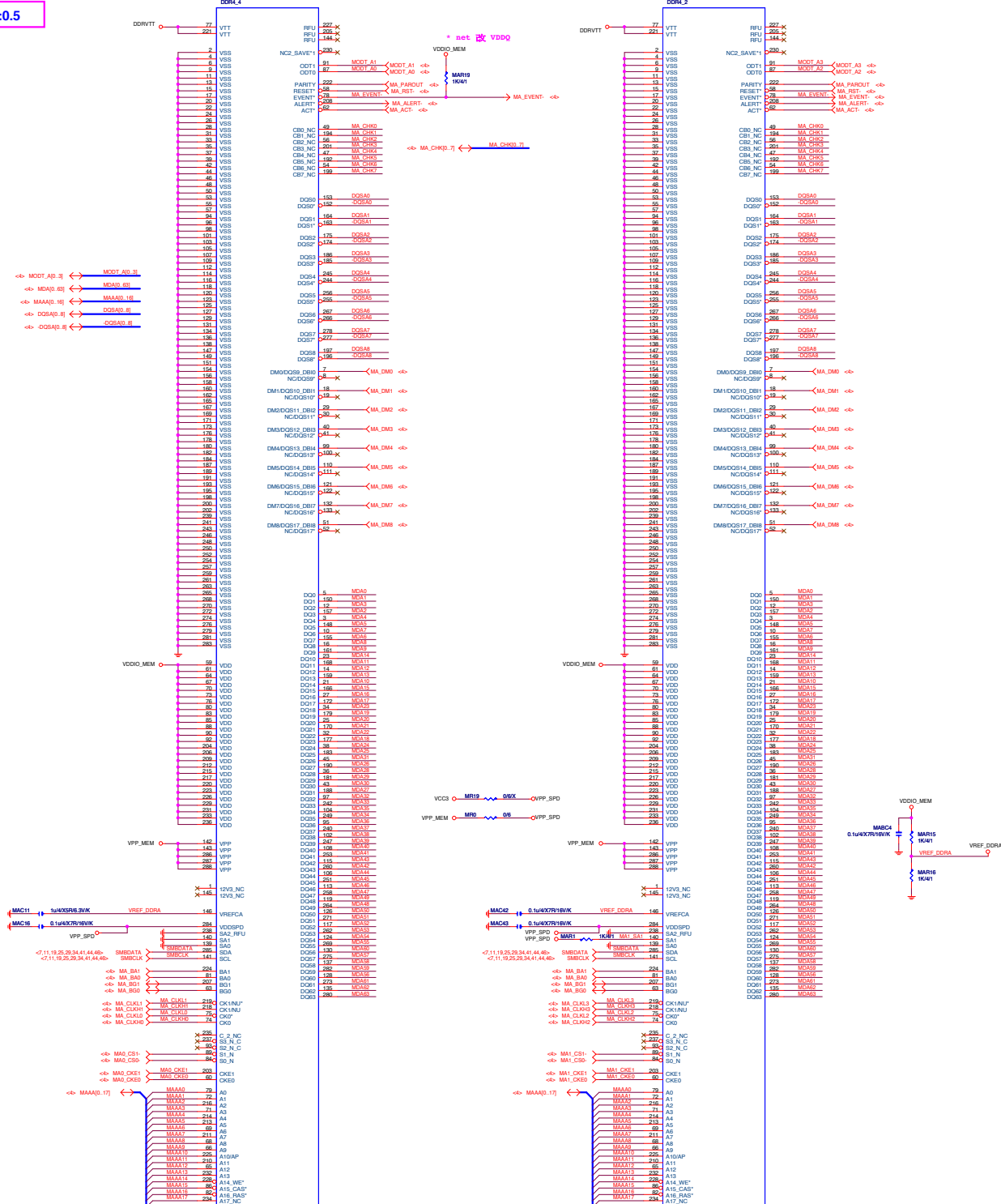




CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN







USB port power control 13:0 (VCC3). Output.

<31> -USBOC_R1
<17,19> -USBOC_F1

PR62 12.1K/4/1 P_UREXT AE10 UREXT

<33> P_SS_RX2P P_SS_RX2N AB15 USB_SS_RXP0
<33> P_SS_RX2N P_SS_RX2N AC15 USB_SS_RXN0
<33> P_SS_RX1P P_SS_RX1N AC16 USB_SS_RXP1
<33> P_SS_RX1N P_SS_RX1N AB16 USB_SS_RXN1
<33> P_SS_RX0P P_SS_RX0N AC18 USB_SS_RXP2
<33> P_SS_RX0N P_SS_RX0N AC18 USB_SS_RXN2
<33> P_SS_RX3P P_SS_RX3N AC19 USB_SS_RXP3
<33> P_SS_RX3N P_SS_RX3N AB19 USB_SS_RXN3
<33> P_SS_RX4P P_SS_RX4N AC21 USB_SS_RXP4
<33> P_SS_RX4N P_SS_RX4N AB21 USB_SS_RXN4
<33> P_SS_RX5P P_SS_RX5N AF24 USB_SS_RXP5
<33> P_SS_RX5N P_SS_RX5N AE24 USB_SS_RXN5

P_SSP_RX0P AB11 USB_SSP_RXP0
P_SSP_RX0N AA11 USB_SSP_RXN0
P_SSP_RX1P AC13 USB_SSP_RXP1
P_SSP_RX1N AB13 USB_SSP_RXN1

USB 3.1 Gen 1

USB_SS_TXP0 AE16 P_SS_TX2P P_SS_TX2N <33>
USB_SS_TXN0 AE16 P_SS_TX2N P_SS_TX2N <33>
USB_SS_TXP1 AF17 P_SS_TX1P P_SS_TX1N <33>
USB_SS_TXN1 AF17 P_SS_TX1N P_SS_TX1N <33>
USB_SS_TXP2 AF18 P_SS_TX0P P_SS_TX0N <33>
USB_SS_TXN2 AF18 P_SS_TX0N P_SS_TX0N <33>
USB_SS_TXP3 AF20 P_SS_TX3P P_SS_TX3N <33>
USB_SS_TXN3 AF20 P_SS_TX3N P_SS_TX3N <33>
USB_SS_TXP4 AF21 P_SS_TX4P P_SS_TX4N <33>
USB_SS_TXN4 AF21 P_SS_TX4N P_SS_TX4N <33>
USB_SS_TXP5 AF22 P_SS_TX5P P_SS_TX5N <33>
USB_SS_TXN5 AF22 P_SS_TX5N P_SS_TX5N <33>

USB 3.1 Gen 2

USB_SSP_TXP0 AE12 P_SSP_TX0P P_SSP_TX0N
USB_SSP_TXN0 AE12 P_SSP_TX0N P_SSP_TX0N
USB_SSP_TXP1 AE14 P_SSP_TX1P P_SSP_TX1N
USB_SSP_TXN1 AE14 P_SSP_TX1N P_SSP_TX1N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

USB31_I211 Lan

F_USB1

F_USB2

F_USB2

F_USB1

USB31_I211 Lan

F_USB30_2

F_USB30_2

USB30_Killer Lan

USB30_Killer Lan

F_USB30_1

F_USB30_1

HSD 6

F_USB30_1

HSD 11

HSD 10

HSD 7

HSD 8

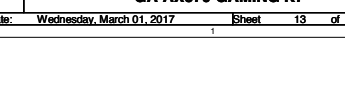
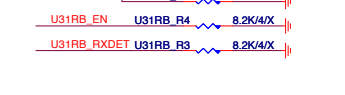
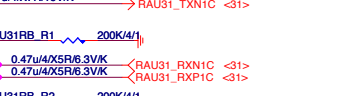
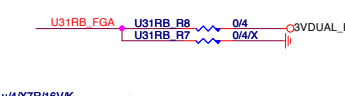
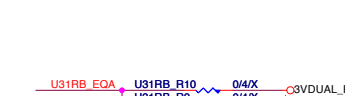
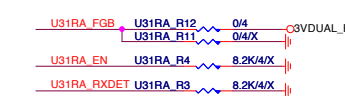
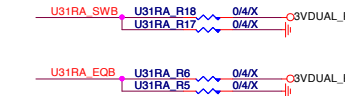
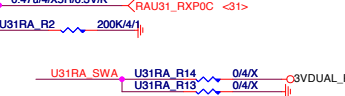
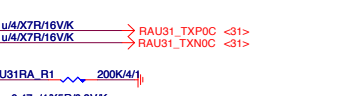
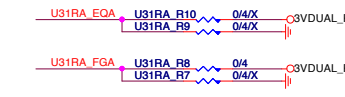
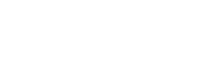
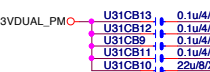
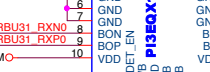
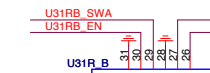
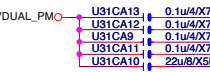
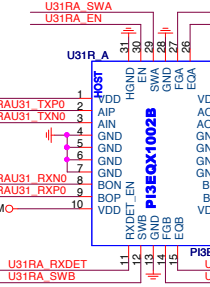
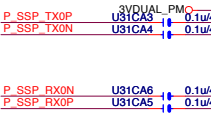
HSD 9

USB30_Killer Lan

HSD 5

USB31_I211 Lan

HSD 0



ANS 5168420

GIGABYTETM

Title

PM USB

Size

Document Number

Custom

GA-AX370-GAMING K7

Rev

1.0

Date

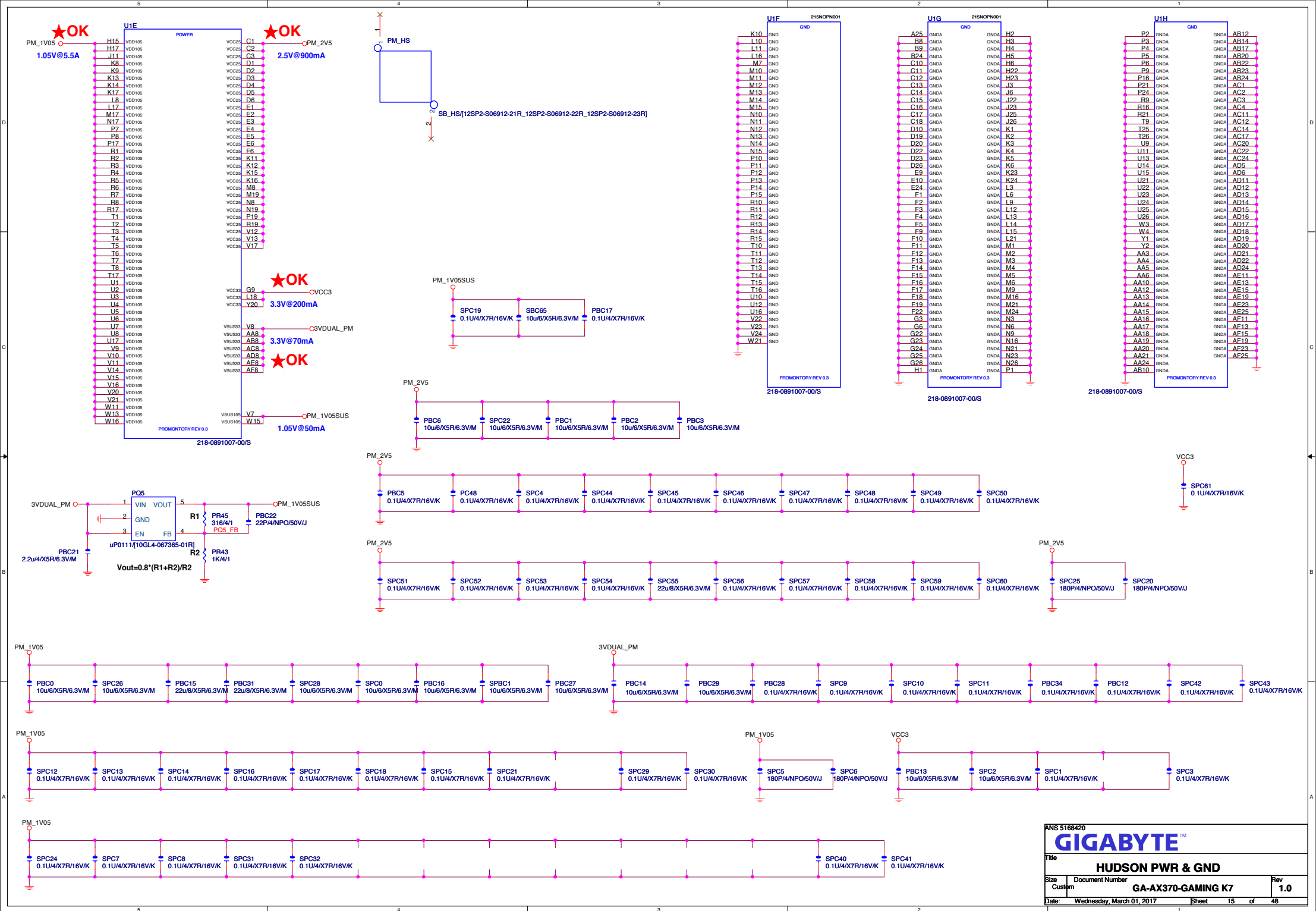
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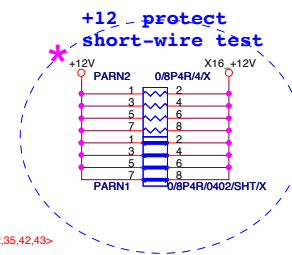
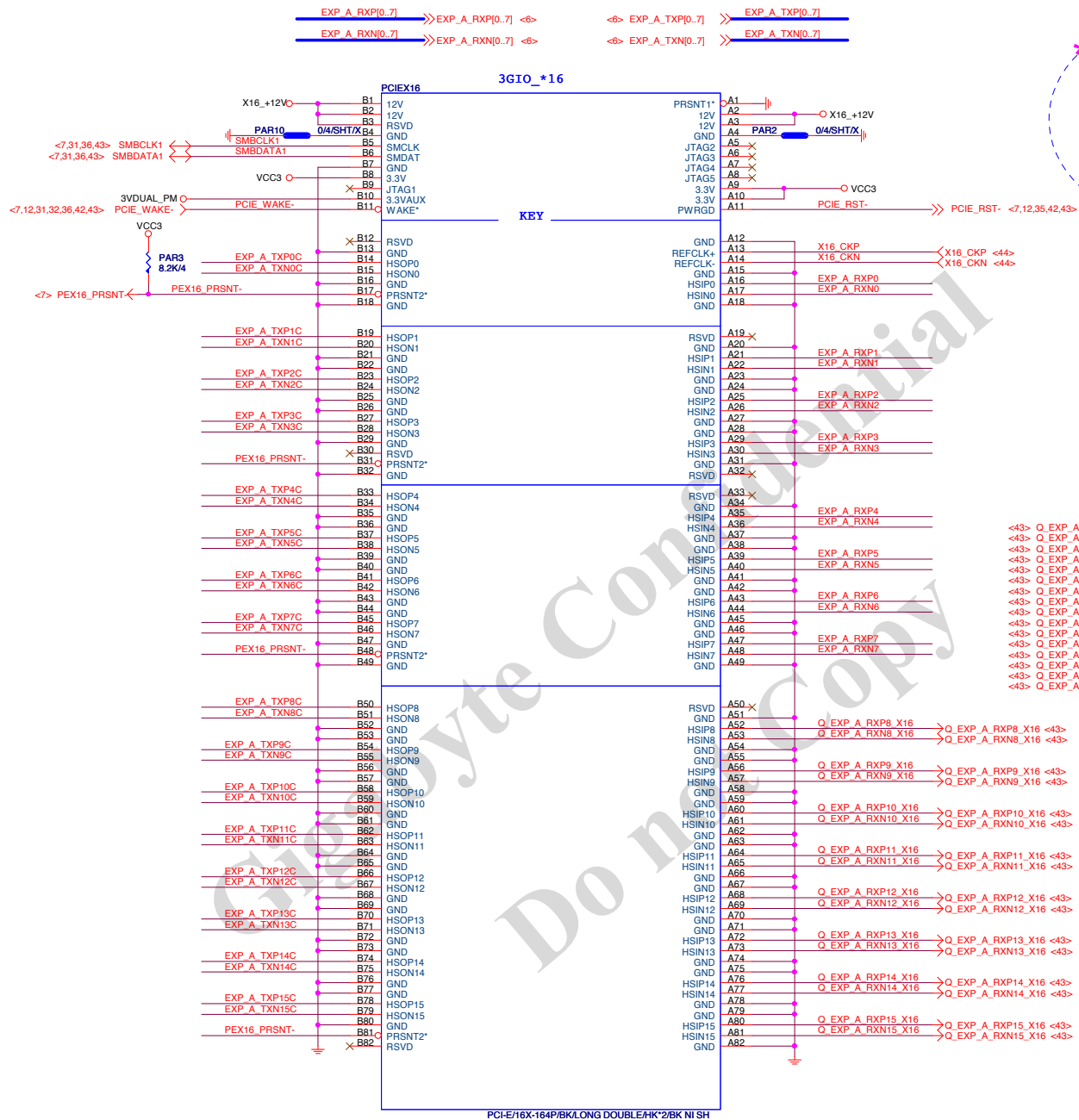
Sheet

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of

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EXP A_TXP0	PAC4	0.22u4/X5R/6.3V/K	EXP A_TXP0C
EXP A_TXN0	PAC5	0.22u4/X5R/6.3V/K	EXP A_TXN0C
EXP A_TXP1	PAC6	0.22u4/X5R/6.3V/K	EXP A_TXP1C
EXP A_TXN1	PAC7	0.22u4/X5R/6.3V/K	EXP A_TXN1C
EXP A_TXP2	PAC8	0.22u4/X5R/6.3V/K	EXP A_TXP2C
EXP A_TXN2	PAC9	0.22u4/X5R/6.3V/K	EXP A_TXN2C
EXP A_TXP3	PAC10	0.22u4/X5R/6.3V/K	EXP A_TXP3C
EXP A_TXN3	PAC11	0.22u4/X5R/6.3V/K	EXP A_TXN3C
EXP A_TXP4	PAC12	0.22u4/X5R/6.3V/K	EXP A_TXP4C
EXP A_TXN4	PAC13	0.22u4/X5R/6.3V/K	EXP A_TXN4C
EXP A_TXP5	PAC14	0.22u4/X5R/6.3V/K	EXP A_TXP5C
EXP A_TXN5	PAC15	0.22u4/X5R/6.3V/K	EXP A_TXN5C
EXP A_TXP6	PAC16	0.22u4/X5R/6.3V/K	EXP A_TXP6C
EXP A_TXN6	PAC17	0.22u4/X5R/6.3V/K	EXP A_TXN6C
EXP A_TXP7	PAC18	0.22u4/X5R/6.3V/K	EXP A_TXP7C
EXP A_TXN7	PAC19	0.22u4/X5R/6.3V/K	EXP A_TXN7C
<43> Q EXP A_TXP8_X16	PAC20	0.22u4/X5R/6.3V/K	EXP A_TXP8C
<43> Q EXP A_TXN8_X16	PAC21	0.22u4/X5R/6.3V/K	EXP A_TXN8C
<43> Q EXP A_TXP9_X16	PAC22	0.22u4/X5R/6.3V/K	EXP A_TXP9C
<43> Q EXP A_TXN9_X16	PAC23	0.22u4/X5R/6.3V/K	EXP A_TXN9C
<43> Q EXP A_TXP10_X16	PAC24	0.22u4/X5R/6.3V/K	EXP A_TXP10C
<43> Q EXP A_TXN10_X16	PAC25	0.22u4/X5R/6.3V/K	EXP A_TXN10C
<43> Q EXP A_TXP11_X16	PAC26	0.22u4/X5R/6.3V/K	EXP A_TXP11C
<43> Q EXP A_TXN11_X16	PAC27	0.22u4/X5R/6.3V/K	EXP A_TXN11C
<43> Q EXP A_TXP12_X16	PAC28	0.22u4/X5R/6.3V/K	EXP A_TXP12C
<43> Q EXP A_TXN12_X16	PAC29	0.22u4/X5R/6.3V/K	EXP A_TXN12C
<43> Q EXP A_TXP13_X16	PAC30	0.22u4/X5R/6.3V/K	EXP A_TXP13C
<43> Q EXP A_TXN13_X16	PAC31	0.22u4/X5R/6.3V/K	EXP A_TXN13C
<43> Q EXP A_TXP14_X16	PAC32	0.22u4/X5R/6.3V/K	EXP A_TXP14C
<43> Q EXP A_TXN14_X16	PAC33	0.22u4/X5R/6.3V/K	EXP A_TXN14C
<43> Q EXP A_TXP15_X16	PAC34	0.22u4/X5R/6.3V/K	EXP A_TXP15C
<43> Q EXP A_TXN15_X16	PAC35	0.22u4/X5R/6.3V/K	EXP A_TXN15C

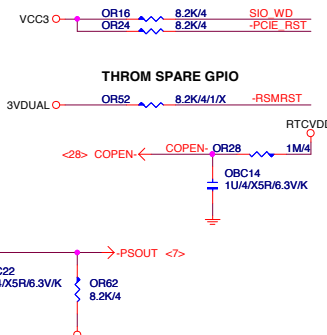


GIGABYTE™

Title: **PCI EXPRESS X 16**

Size: Custom Document Number: **GA-AX370-GAMING K7** Rev: **1.0**

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SIO STRAP

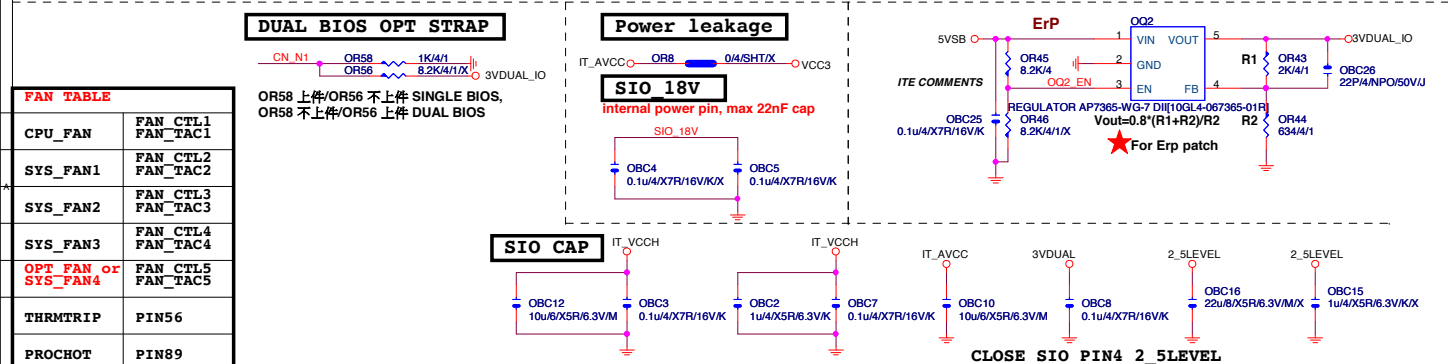


The diagram shows the SIO STRAP pin configuration. On the left, three pins are labeled OR33, OR81, and OR80, each with a 1K4/H resistor connected to ground. On the right, seven pins are labeled JP2, JP3, JP4, JP5, JP6, JP7, and JP8, each with a 8.2K/4 resistor connected to VCC3. The pins are also labeled with their internal functions: OR36, OR35, OR32, OR12, and OR37. The connections are as follows: OR33 to JP2, OR81 to JP3, OR80 to JP4, JP5 to JP6, JP7 to JP8, and JP8 to VCC3. The pins are also labeled with their internal functions: OR36, OR35, OR32, OR12, and OR37.

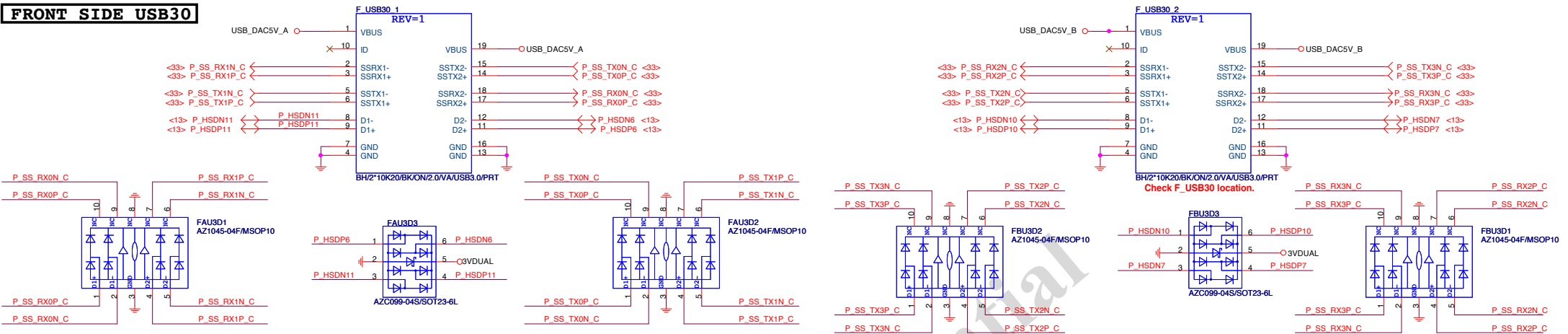
Pin	Resistor	Internal Function	Connection
OR33	1K4/H	OR36	JP2
OR81	1K4/H/H	OR35	JP3
OR80	1K4/H/H	OR32	JP4
JP5	8.2K/4	OR12	JP6
JP7	8.2K/4	OR37	JP8
JP8	8.2K/4		VCC3

JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
JP3	1 0	CE mode 2
	0 0	CE mode 3

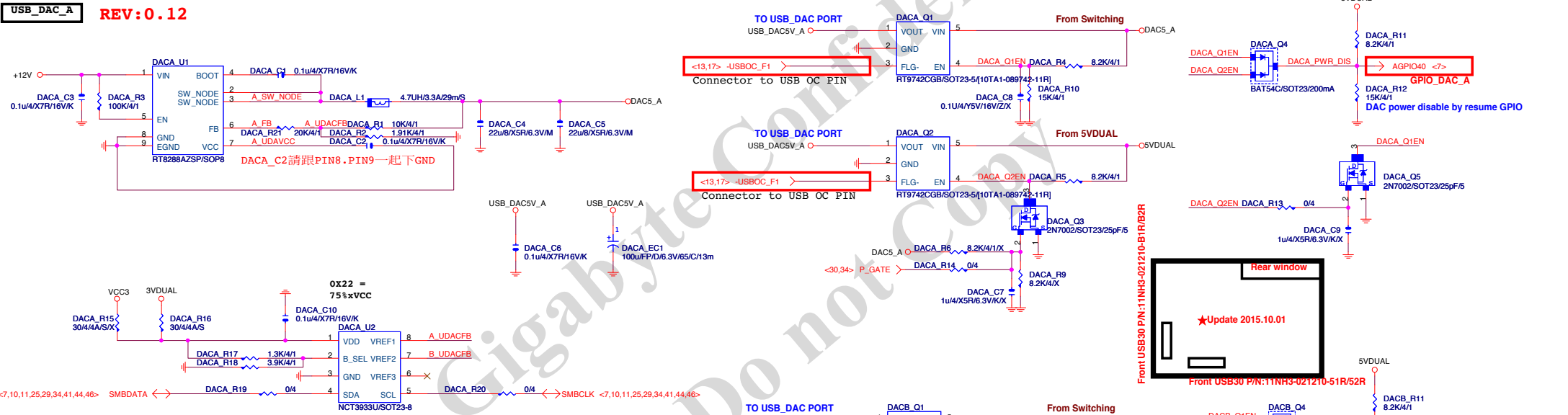
			
Title			
ITE 8686 LPC IO, TPM, KB/MS			
Size	Document Number		Rev
Custom	GA-AX370-GAMING K7		1.0
Date:	Tuesday, February 14, 2017	Sheet	18 of 48



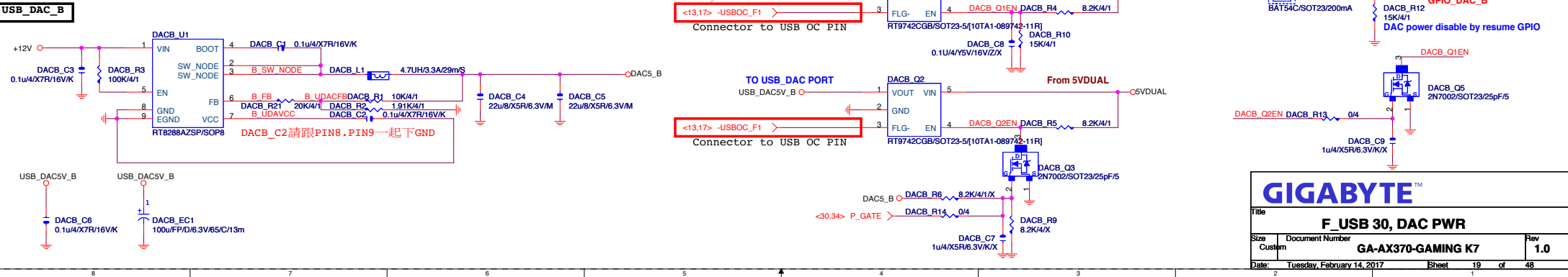
FRONT SIDE USB30



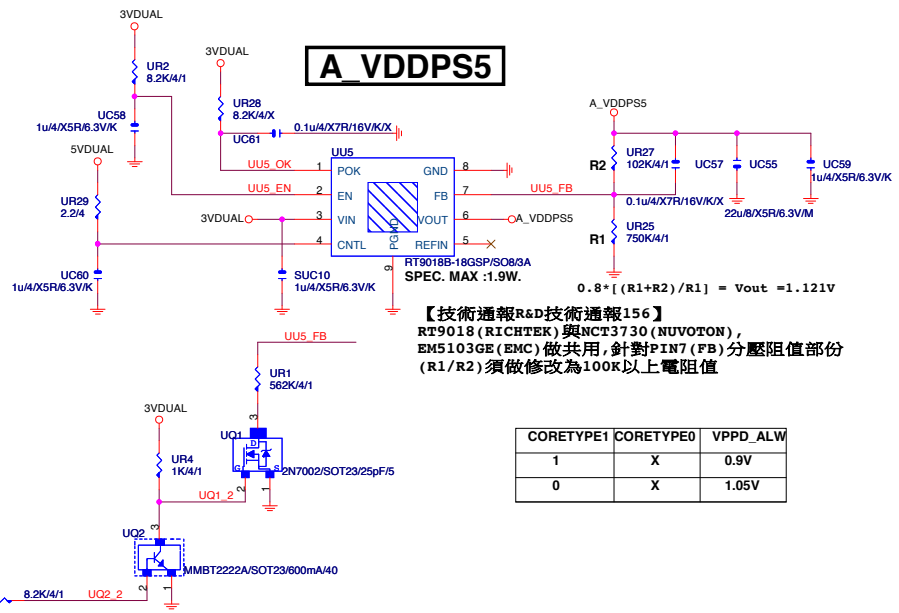
USB_DAC_A REV:0.12



USB_DAC_B



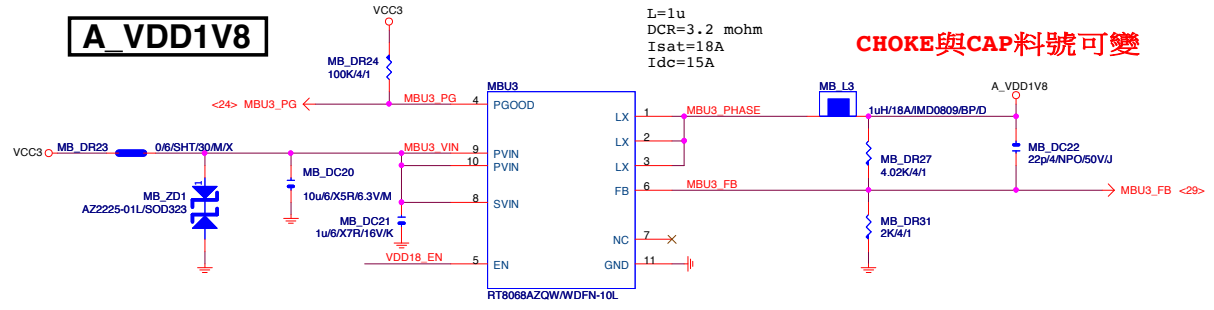
A_VDDPS5



【技術通報R&D技術通報156】
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
(R1/R2) 須做修改為 100K 以上電阻值

REV:0.4

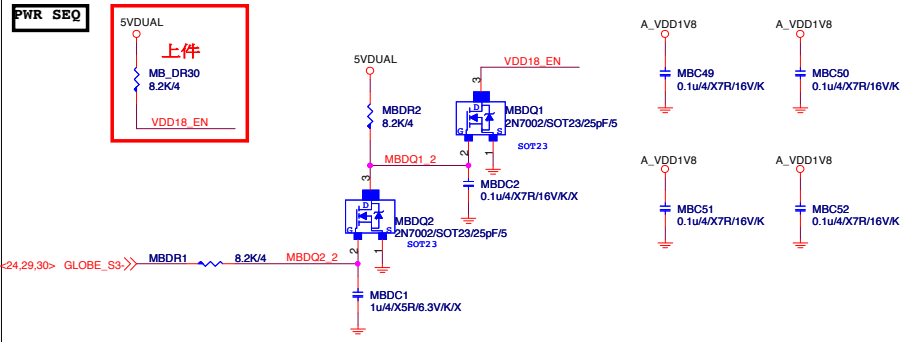
A_VDD1V8



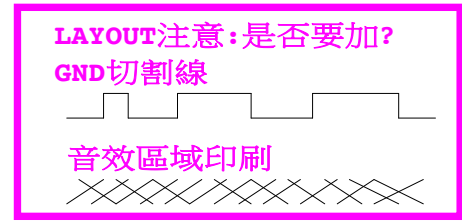
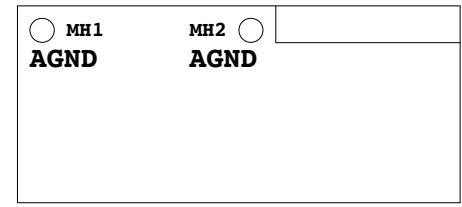
VPP CAP

* 大電容 x0
22u*1PCS

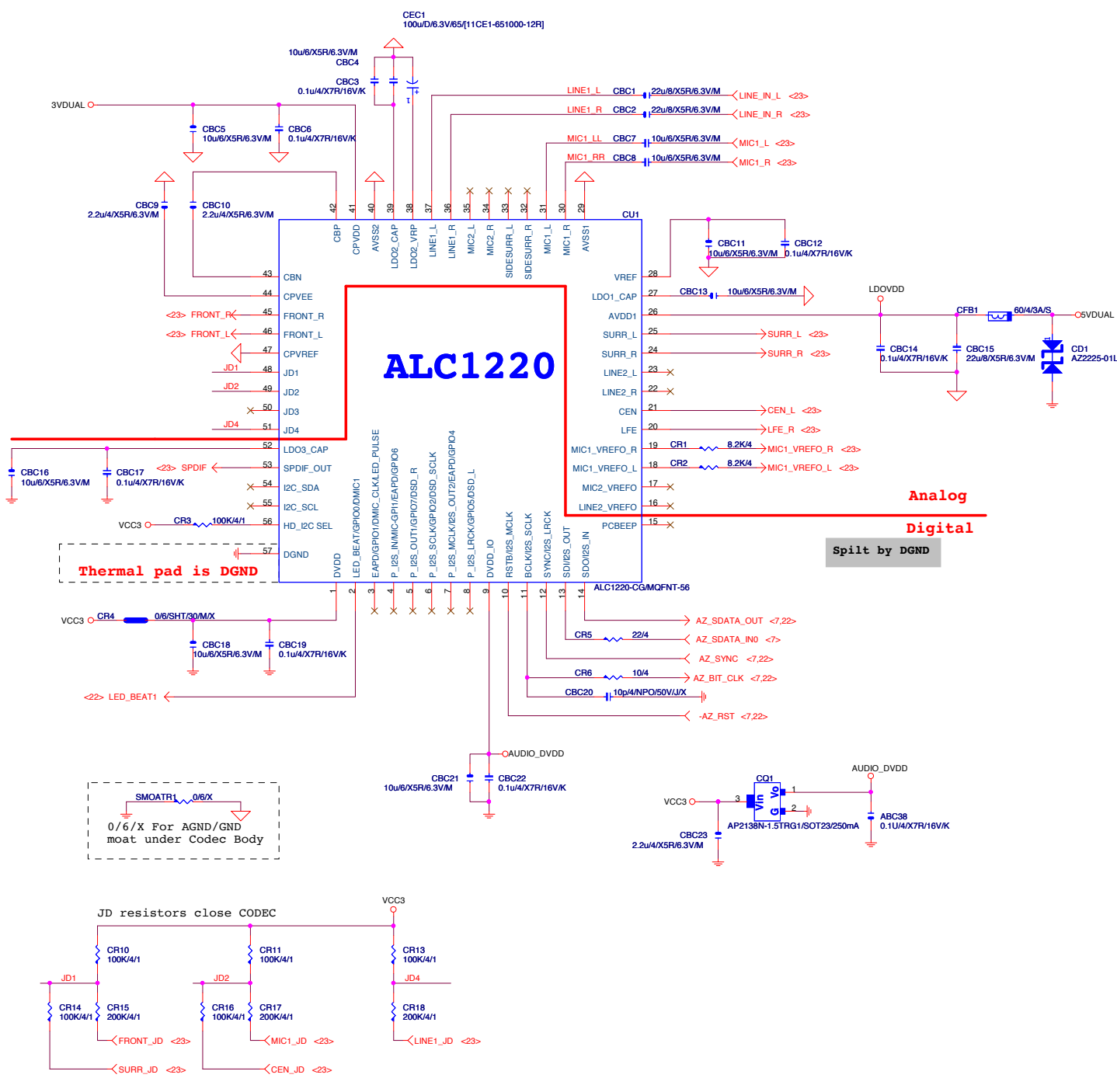
PWR SEQ

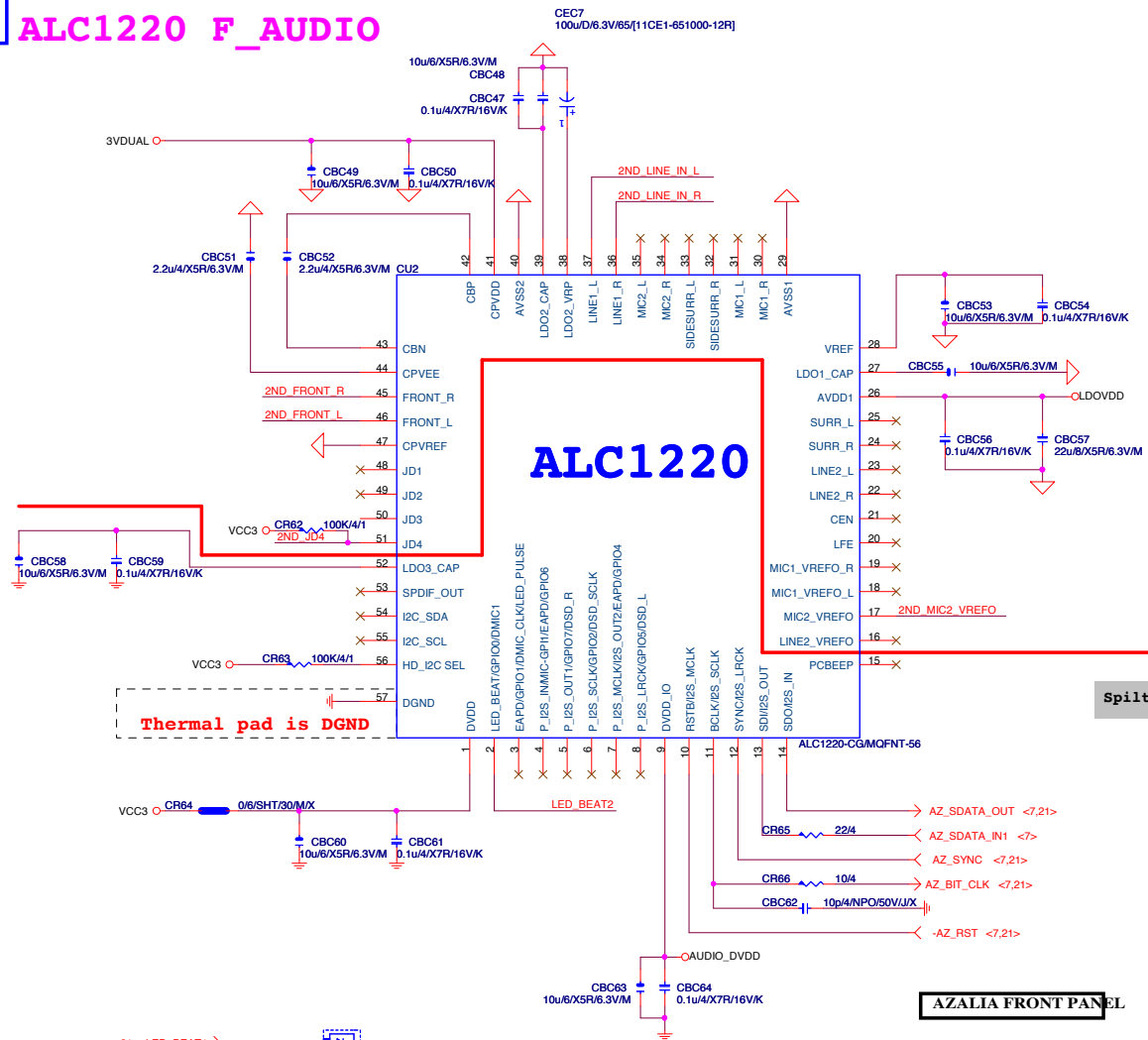


LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
空間不夠,改為Isolate
2. MH2一律改為Isolate

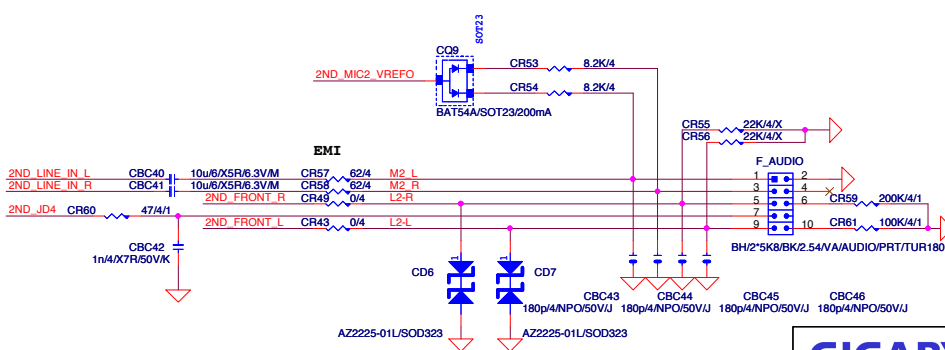


BOM OPTION :
1. AUDIO CONNECT
不銹鋼料號:11NR6-403025-A2R
鍍金料號:11NR6-403025-92R
2. AUDIO CAP
Nichicon MW音效電容 : 11CE1-651000-12R
Chemicon音效電容 : 11CE2-651000-05R



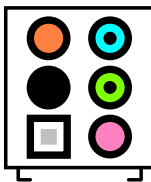


AZALIA FRONT PANEL

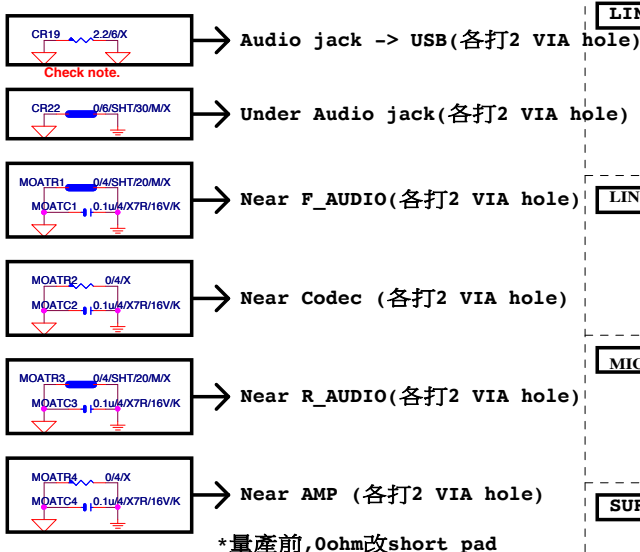
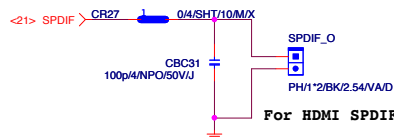


Rev 0.1

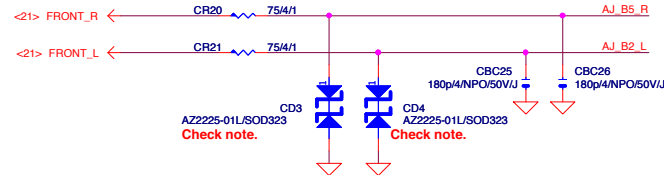
AZALIA JACK



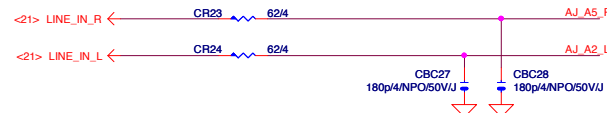
SPDIF_OUT



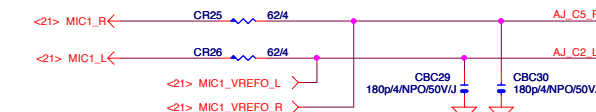
LINE-OUT



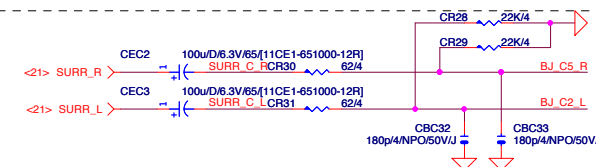
LINE-IN



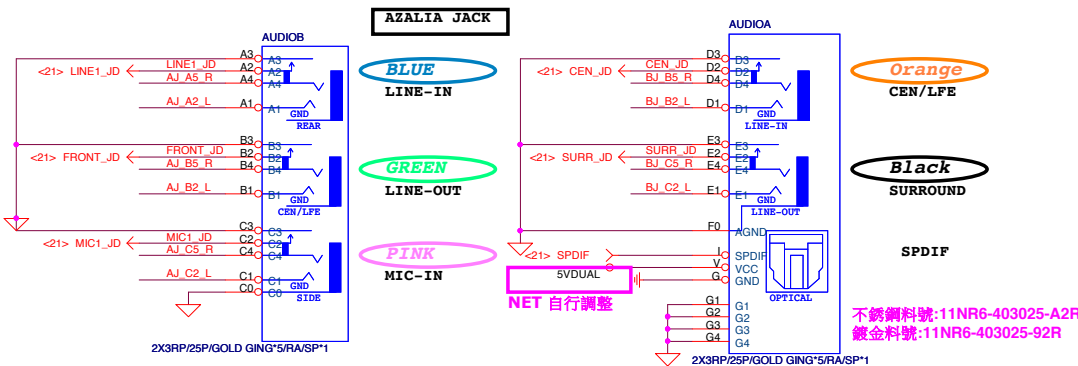
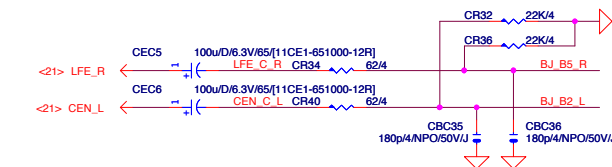
MIC-IN



SURROUND



CEN/LFE

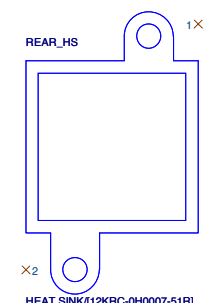


Orange
CEN/LFE

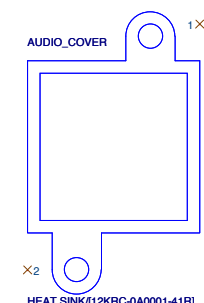
Black
SURROUND

SPDIF

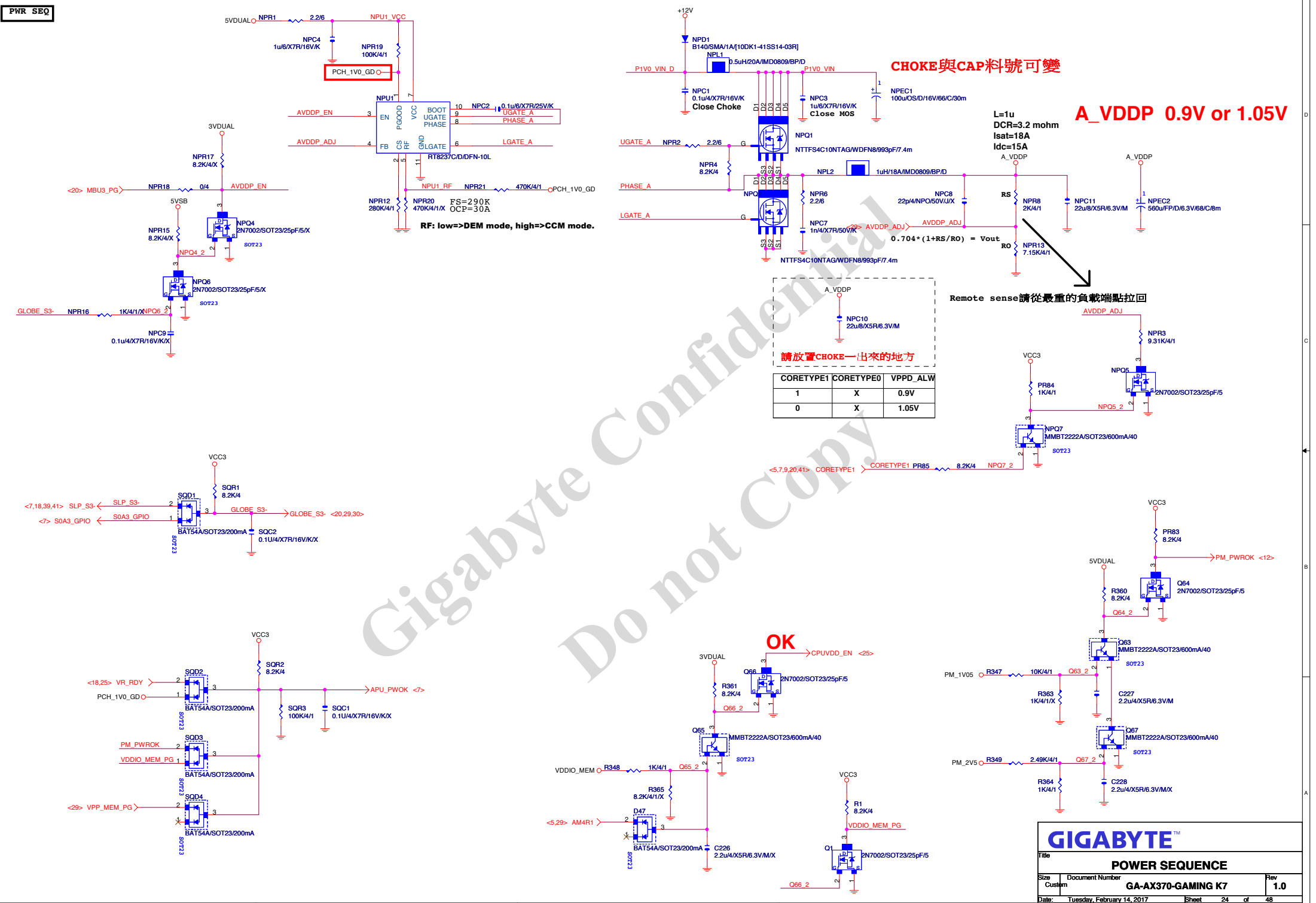
不銹鋼料號:11NR6-403025-A2R
鍍金料號:11NR6-403025-92R

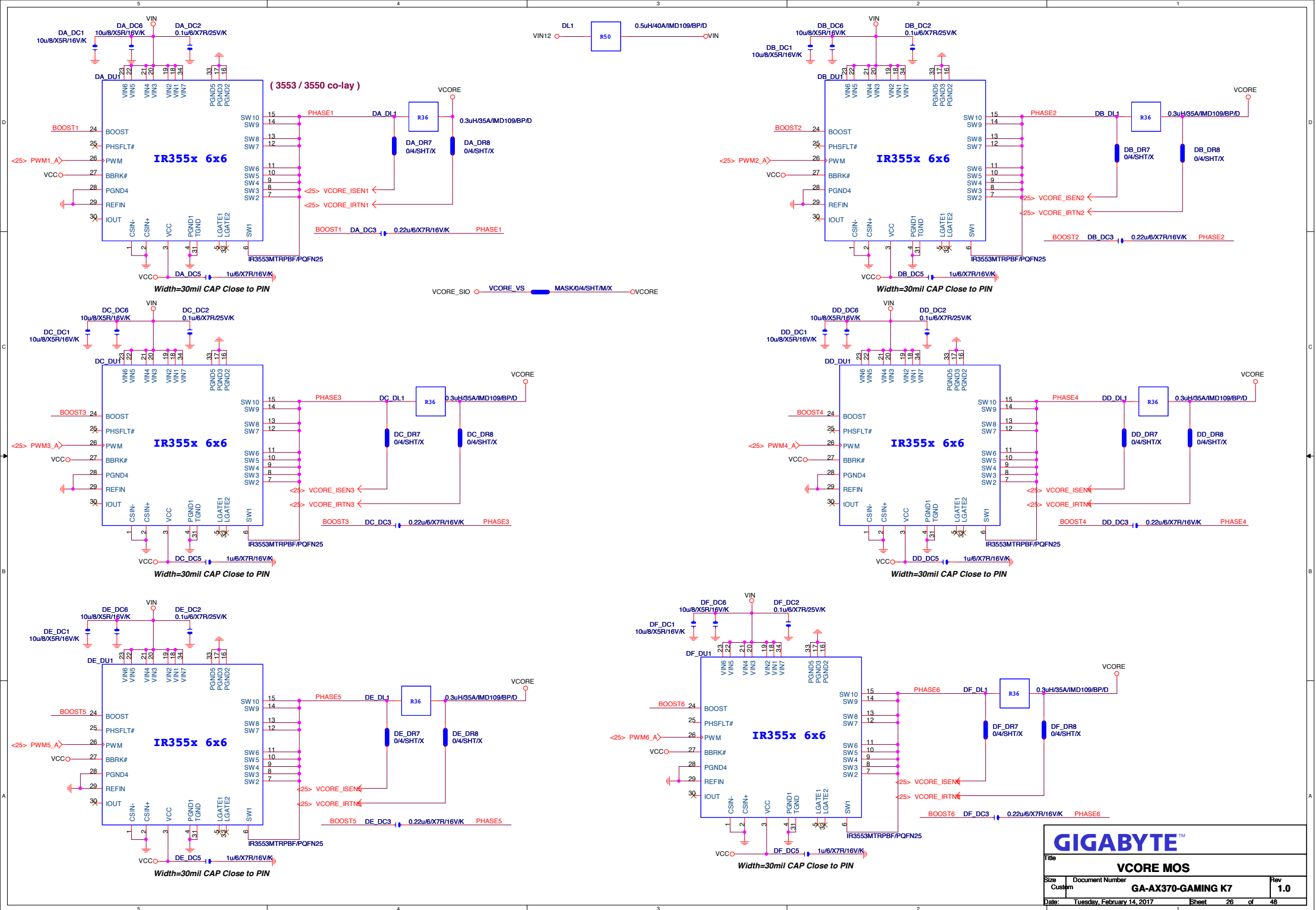


Footprint "Z270X_BASE_COVER"

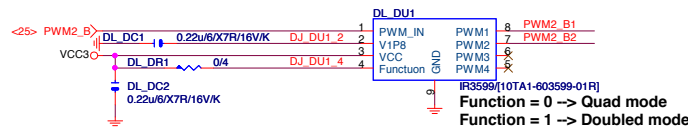
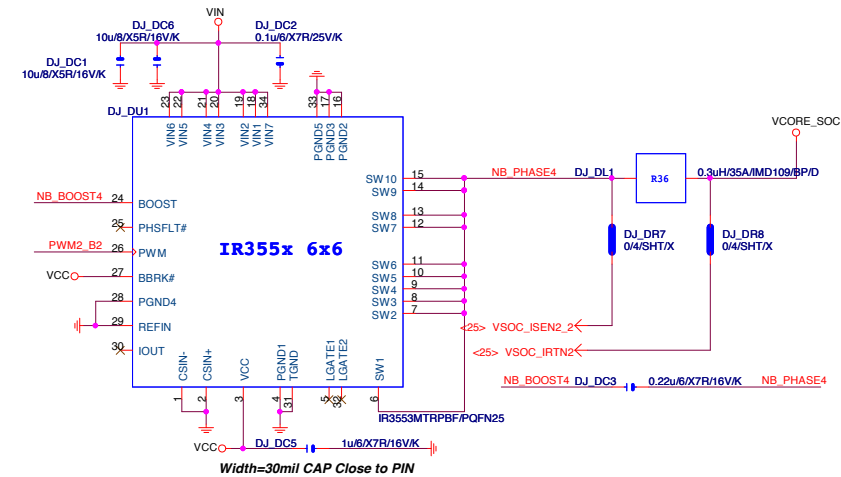
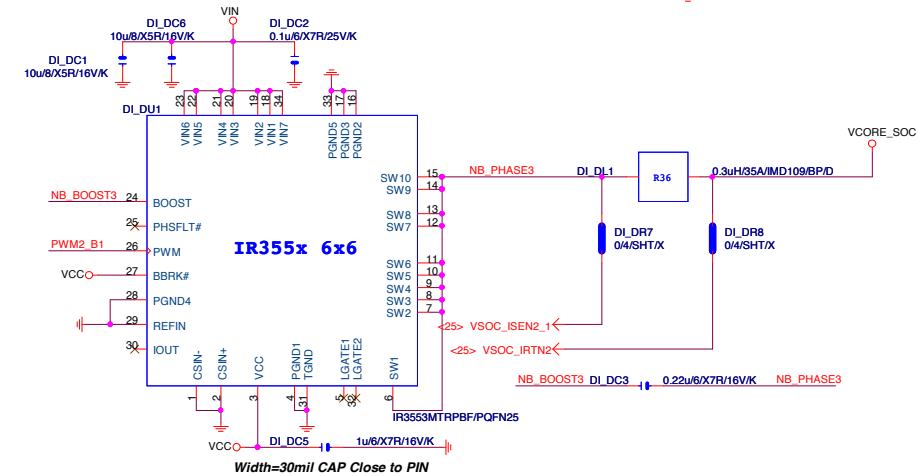
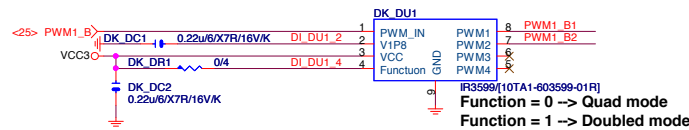
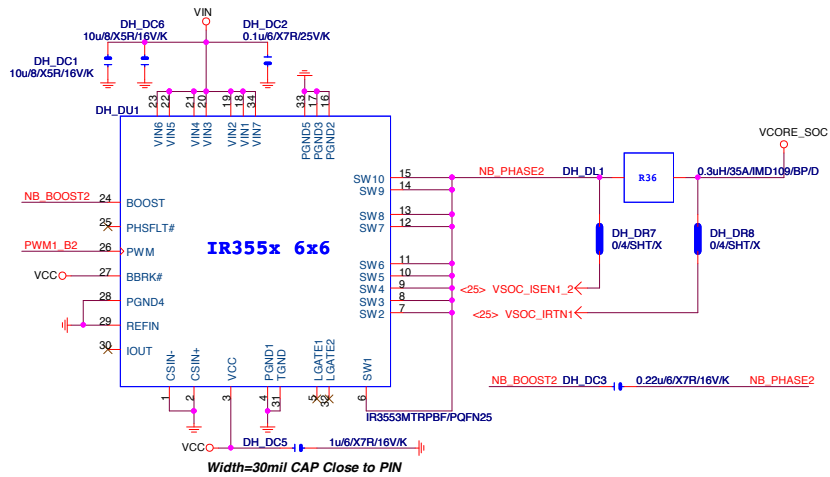
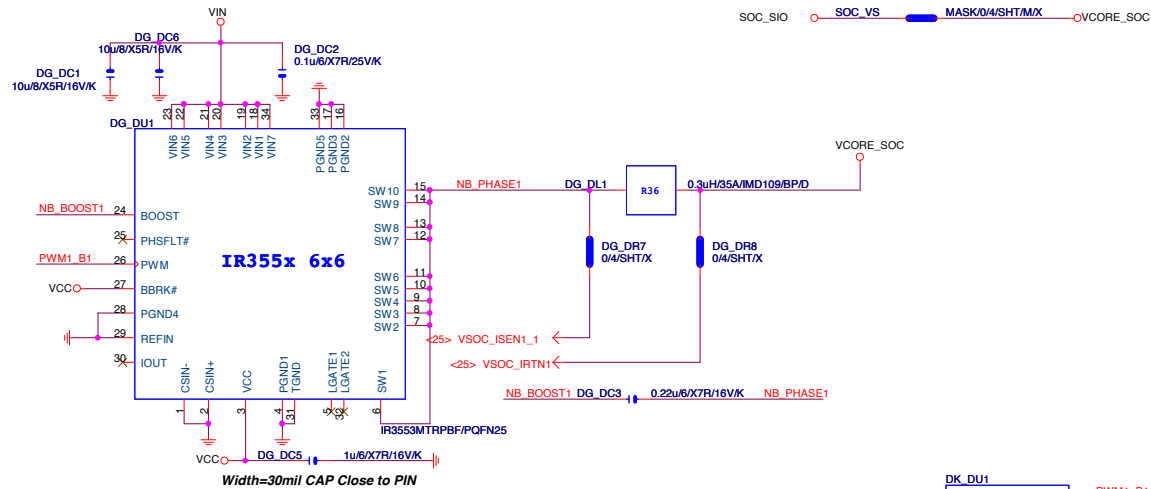


Footprint "Z270X_EXTEND_COVER"

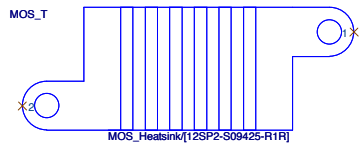
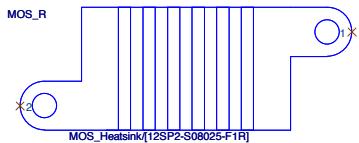




Vcore_Soc



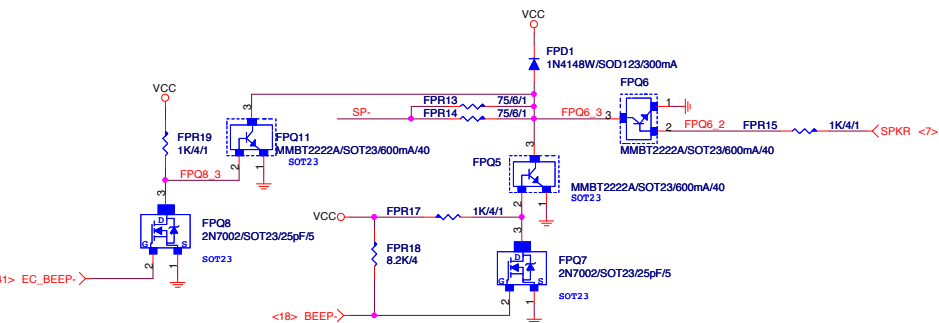
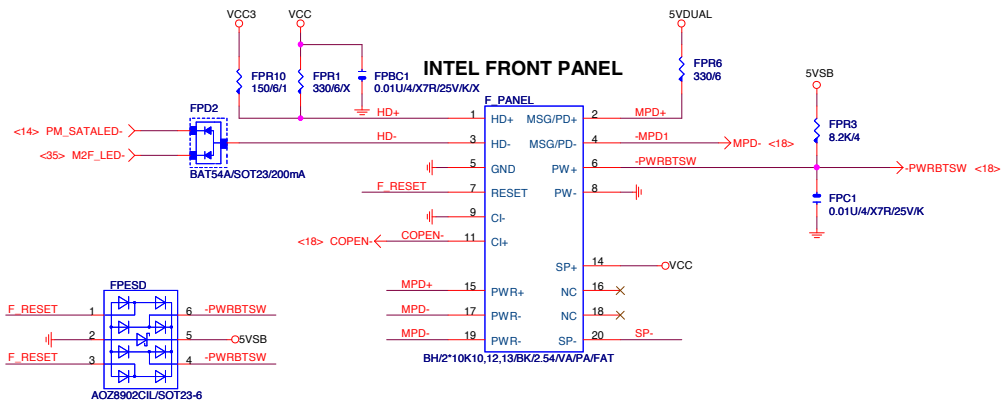
MOS HEATSINK



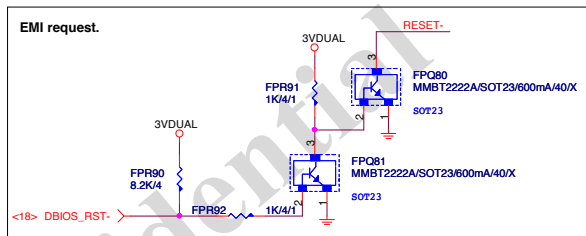
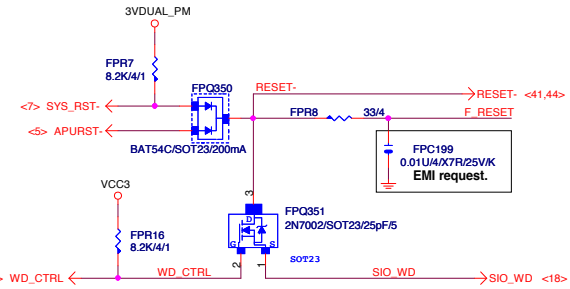
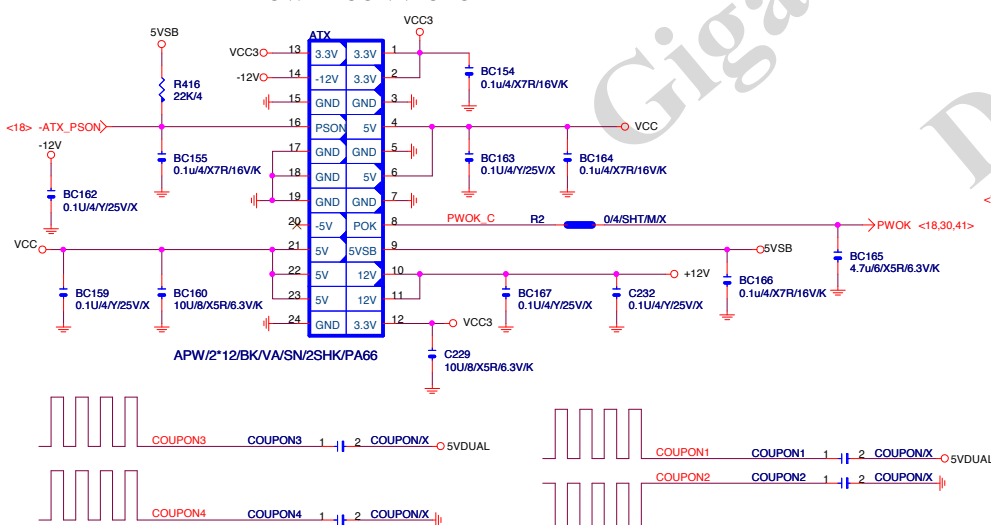
GIGABYTE™

VCORE_SOC		
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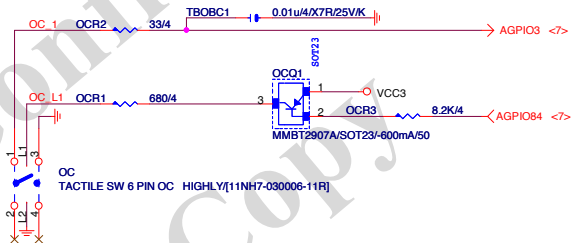
INTEL FRONT PANEL



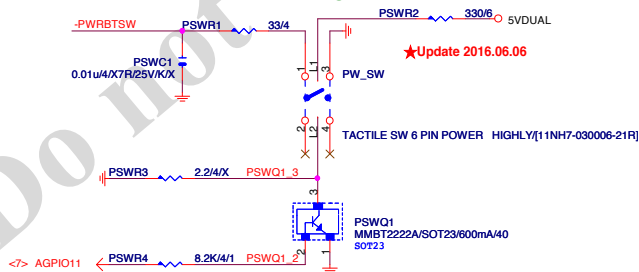
ATX POWER CONNECTOR



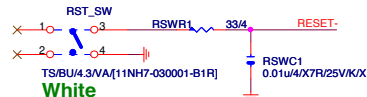
OC KEY



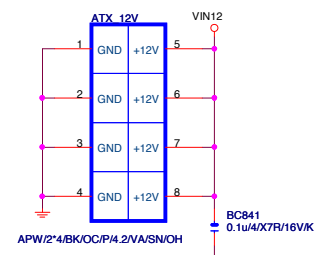
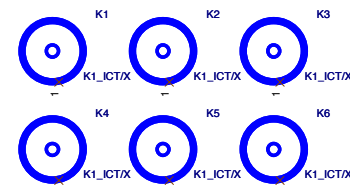
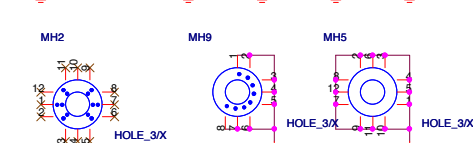
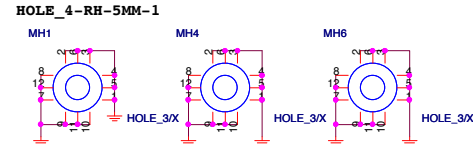
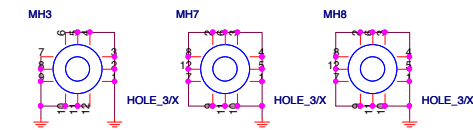
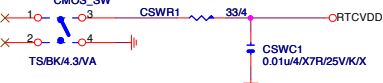
POWER



Reset



Clear CMOS

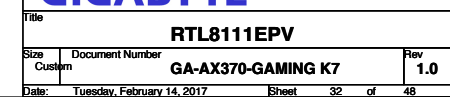


GIGABYTE

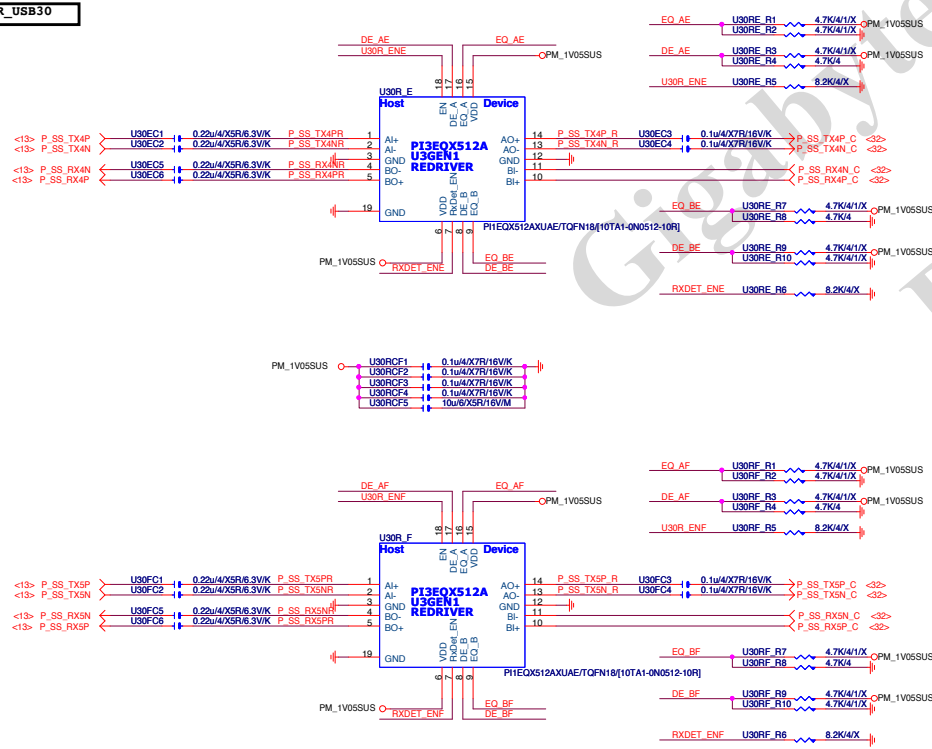
ATX, FRONT PANEL

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Date	Sheet	of
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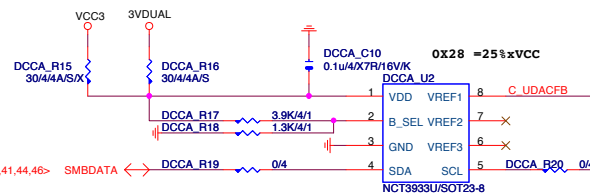
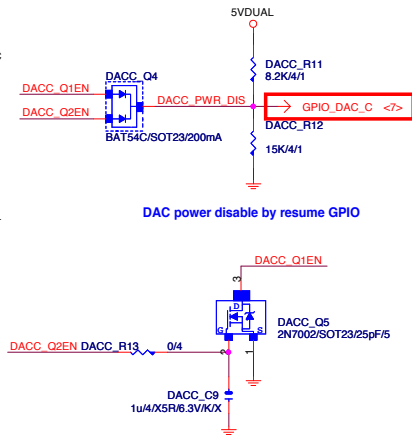
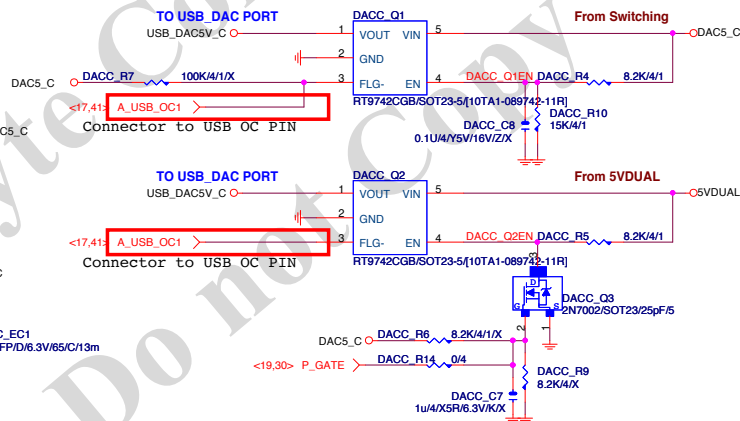
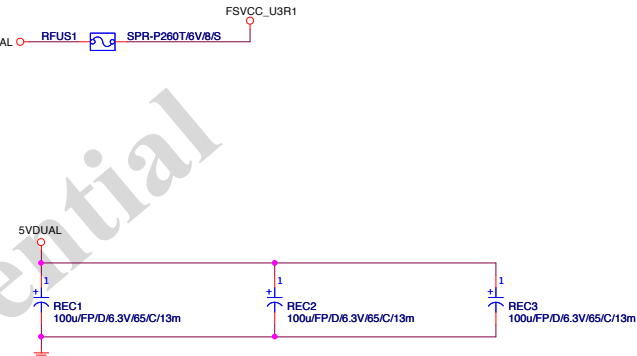
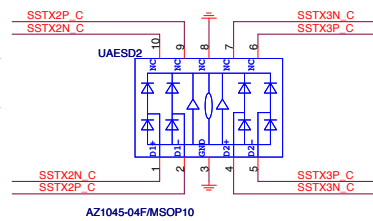
R_USB30



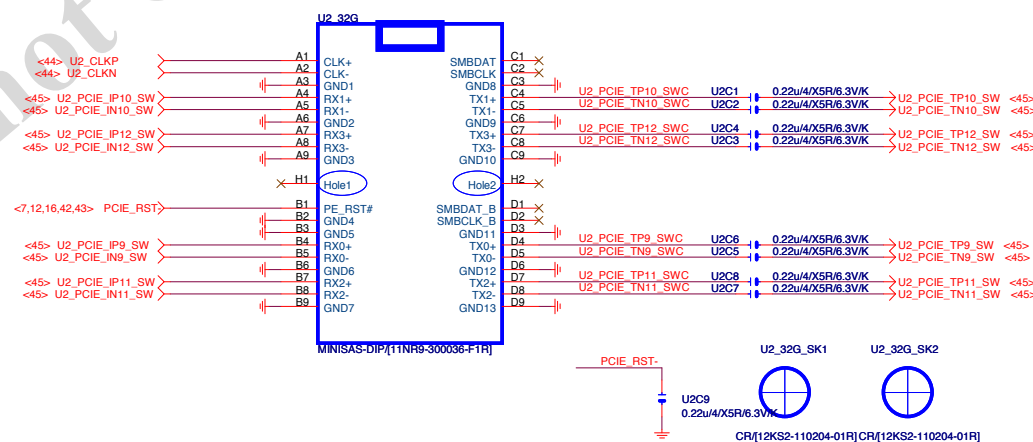
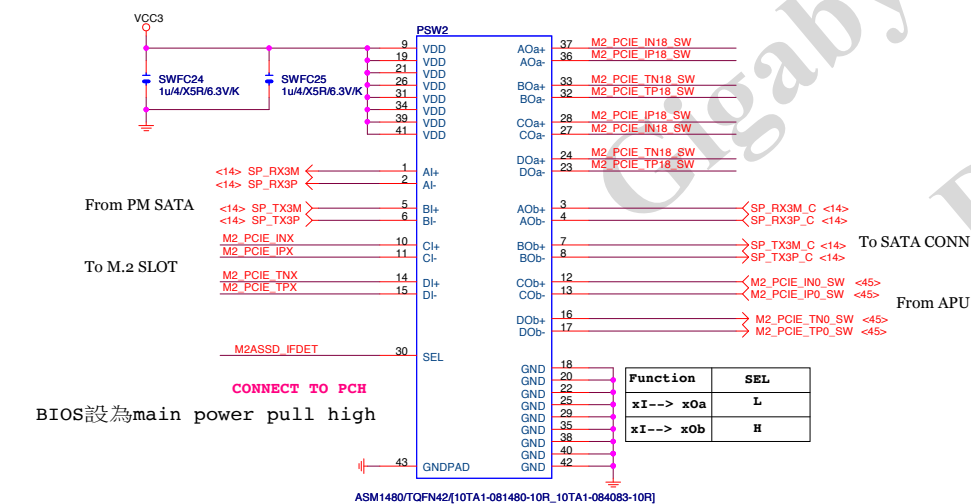
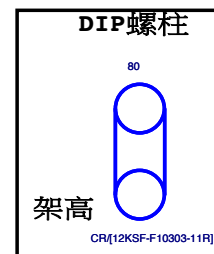
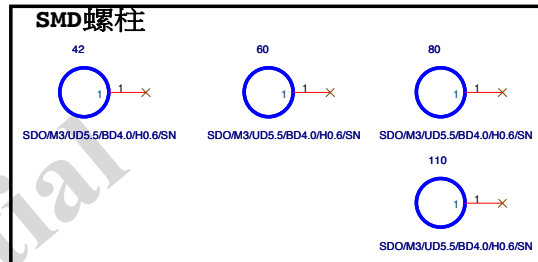
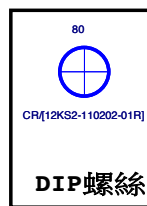
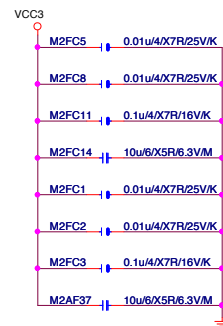
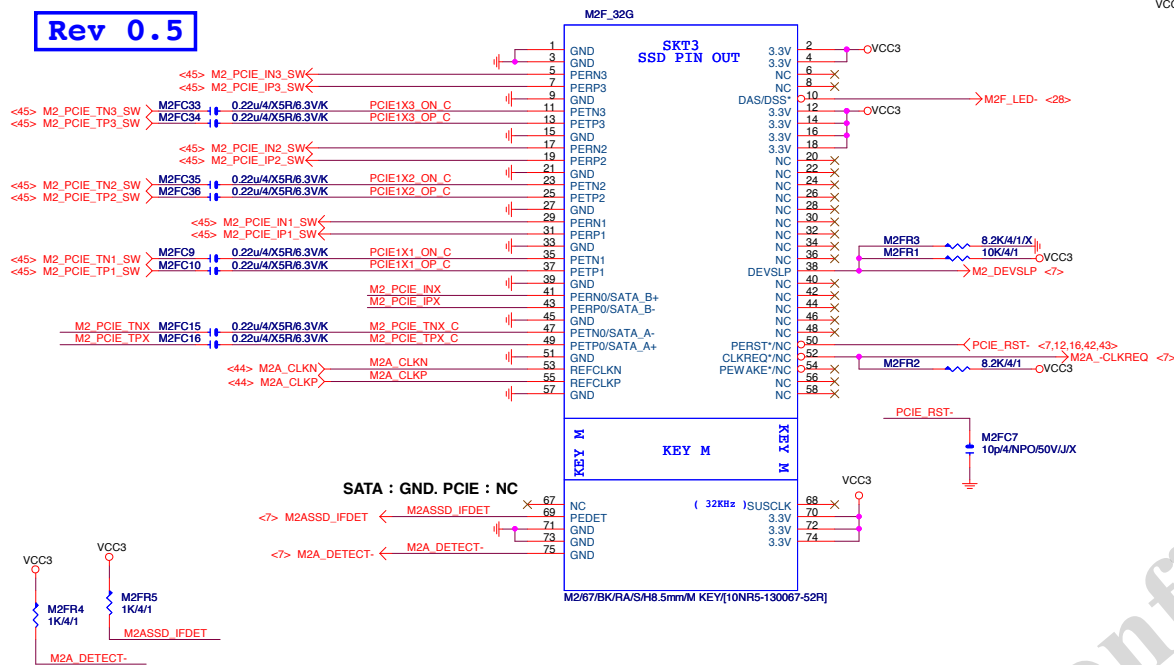
USB_DAC_C

RT8288AZSP/SOP8

DACC_C2請跟PIN8、PIN9一起下GND



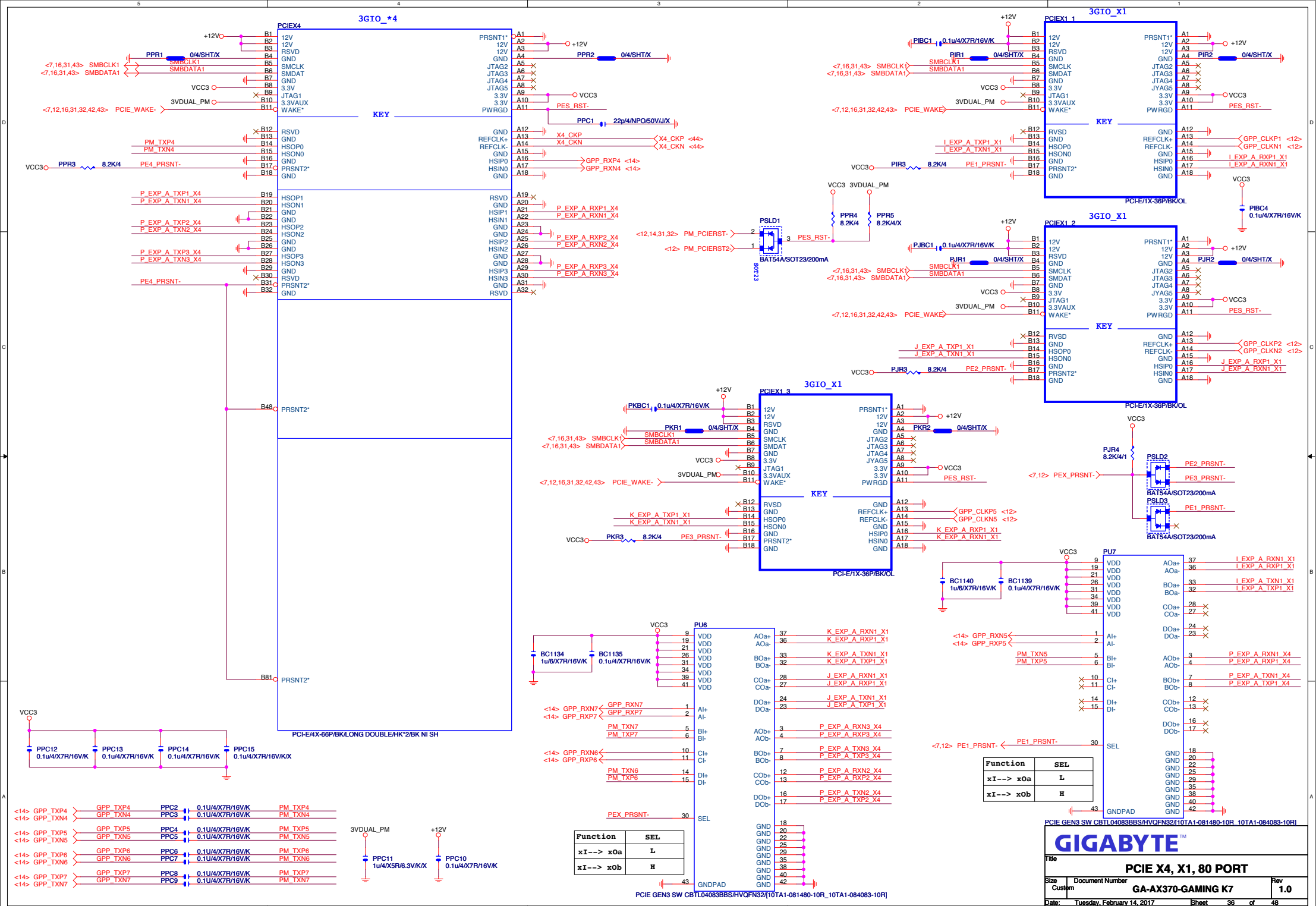
Rev 0.5



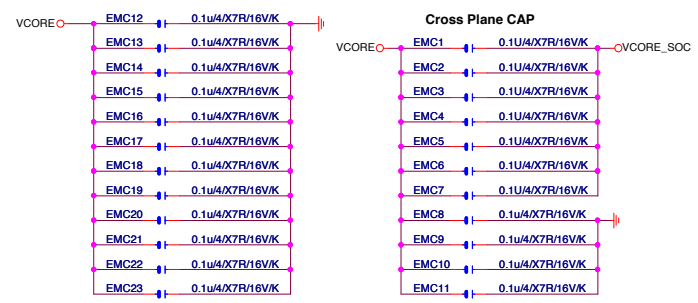
GIGABYTE

Title	U.2, M.2 SOCKET
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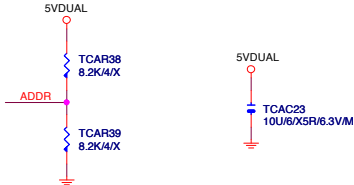
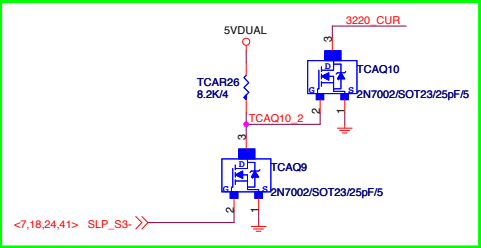
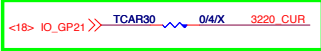
CPU TOP CAVITY



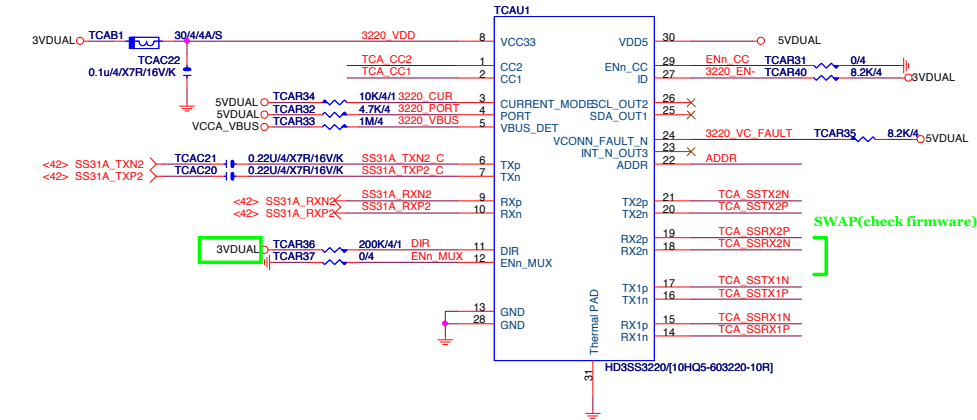
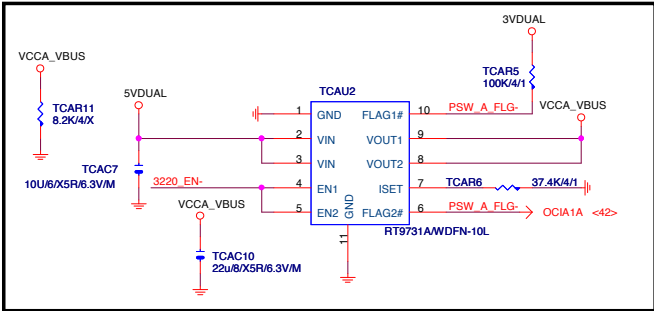


ASM1143 USB31 Host Rev0.3 TI HD3SS3220

For VBUS current limit at 900mA on S3



TypeC default 5V/3A



SWAP(check firmware)

USB 3.1 Red
架高, Lotus.

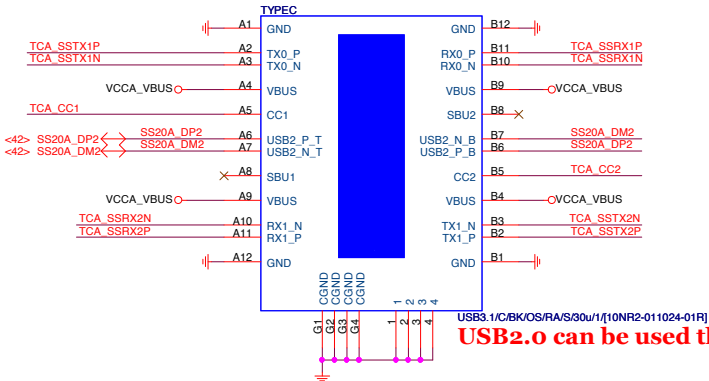


PORT

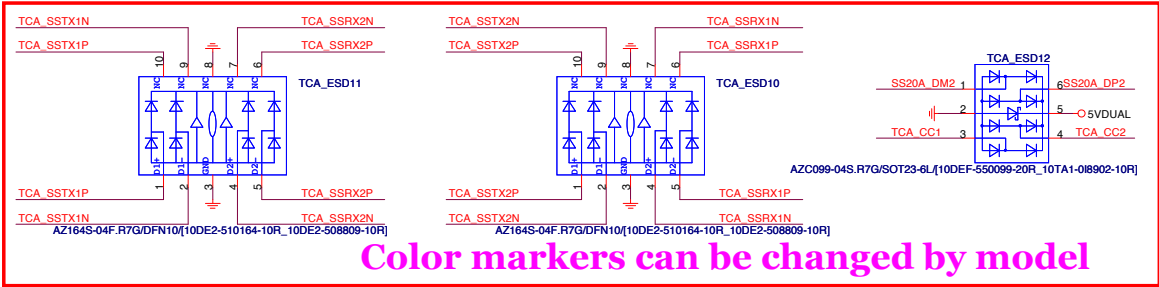
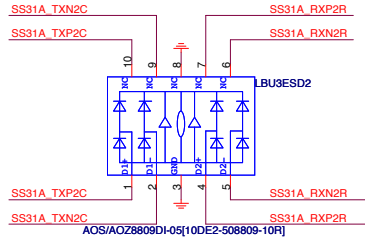
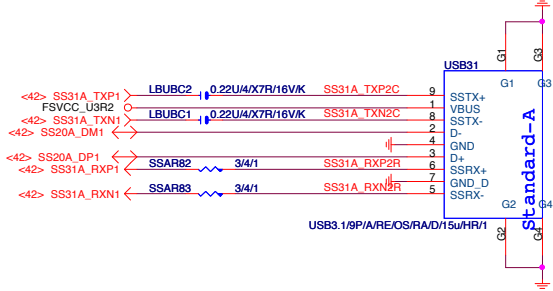
- H - HOST (DFP/SOURCE)
L - Device (UFP/SINK)
NC - Dual Role (DRP)

CURRENT MODE

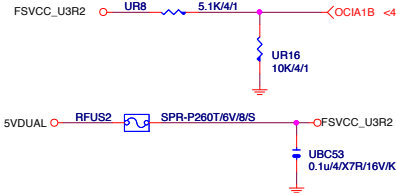
- L - Default (900mA) / Pull down to GND or NC
M - Medium (1.5A) / Pull up to VDD 500K
H - High (3.0A) / Pull up to VDD 10K



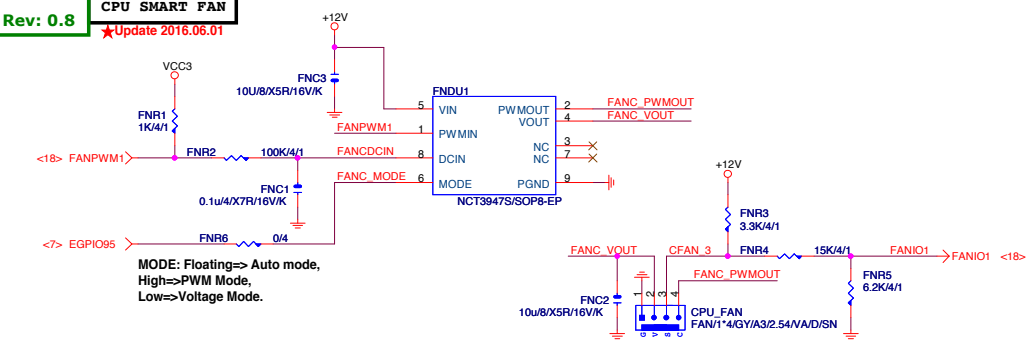
USB2.o can be used the same source



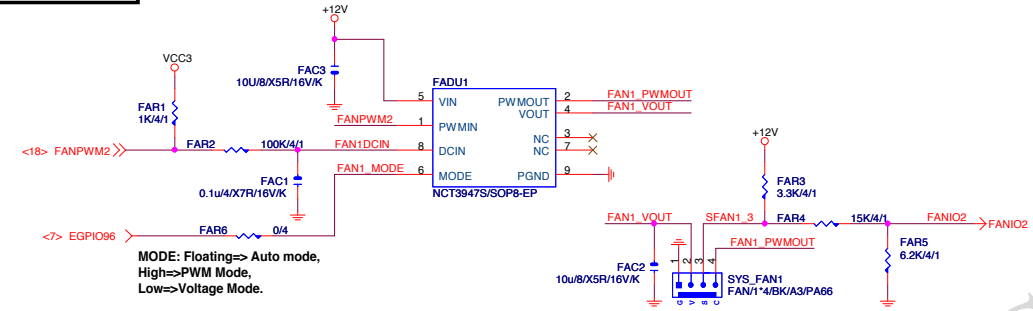
Color markers can be changed by model



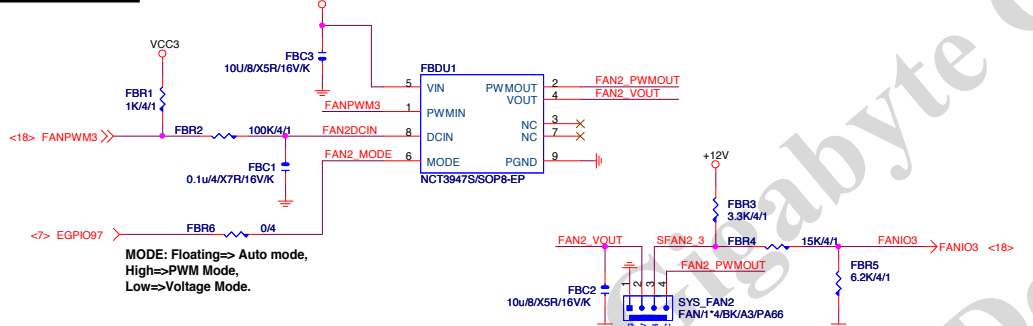
GIGABYTE™		
Title M.2 SOCKET		
Size Custom	Document Number GA-AX370-GAMING K7	Rev 1.0
Date: Tuesday, February 14, 2017 Sheet 39 of 48		



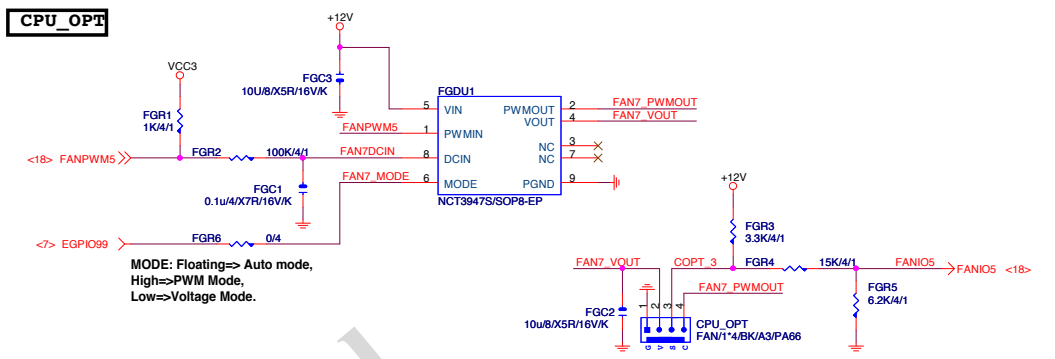
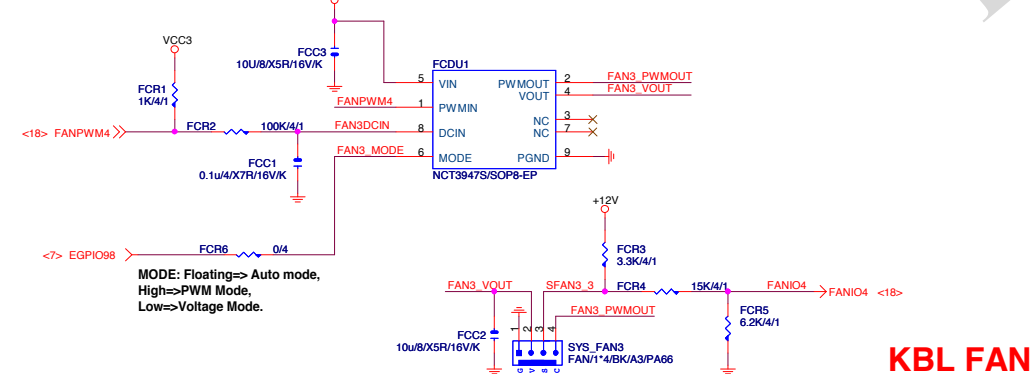
SYSTEM FAN1



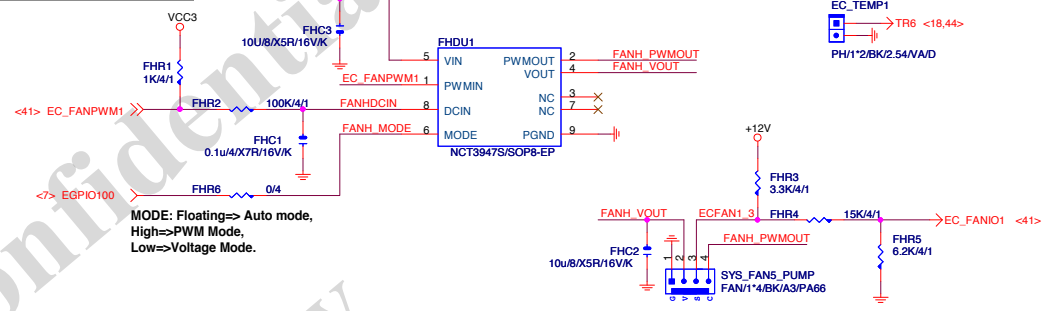
SYSTEM FAN2



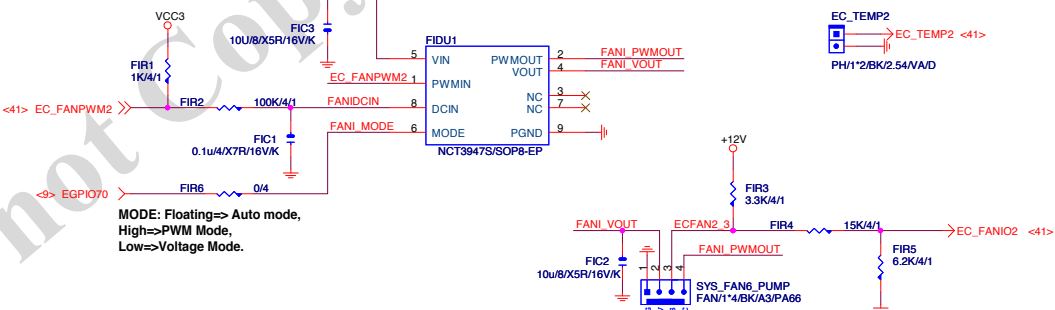
SYSTEM FAN3



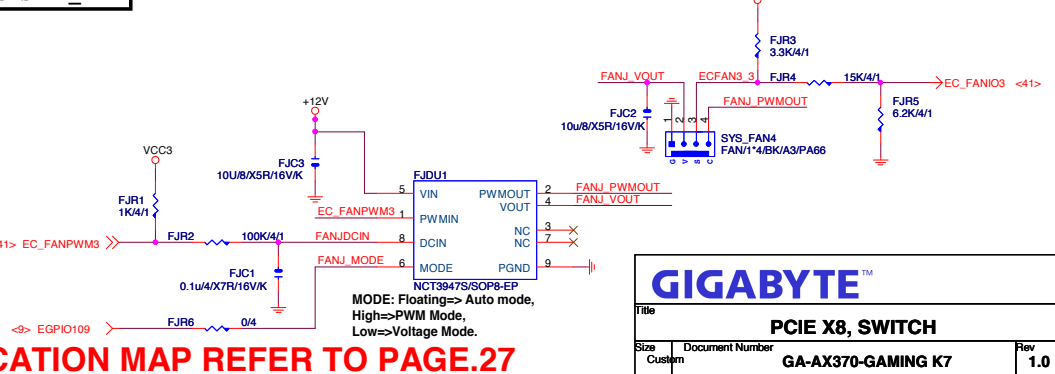
SYSTEM FAN5 PUMP



SYSTEM FAN6 PUMP



SYSTEM FAN4



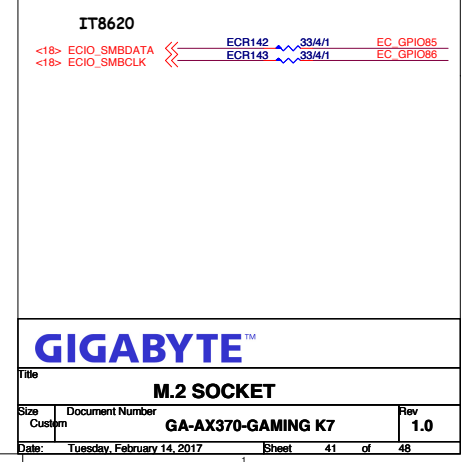
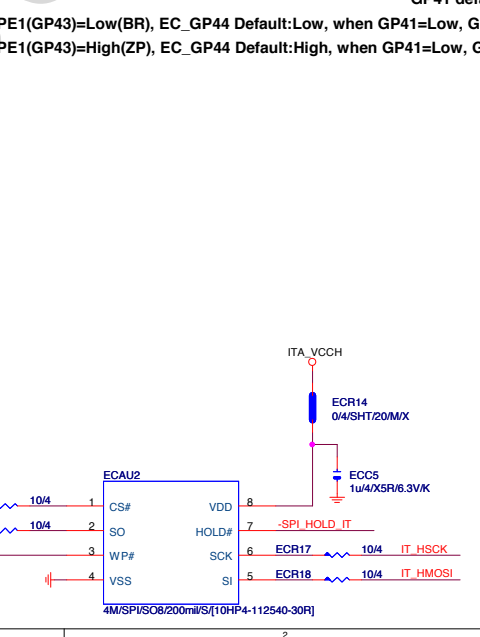
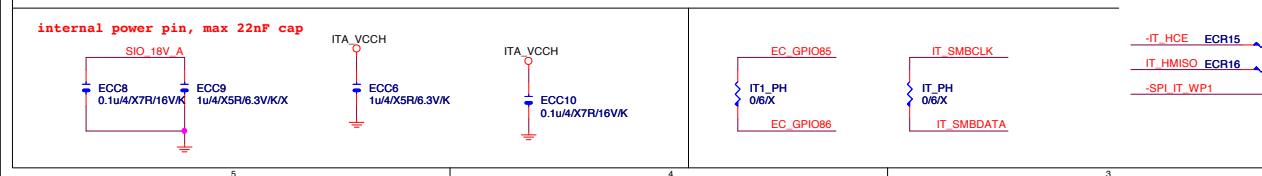
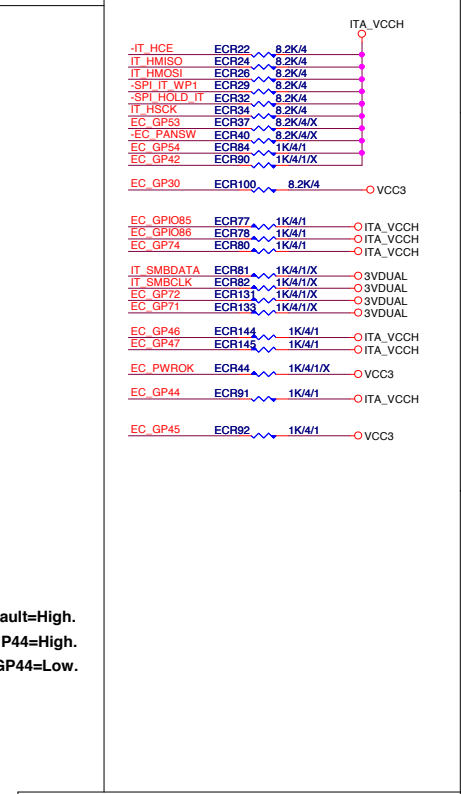
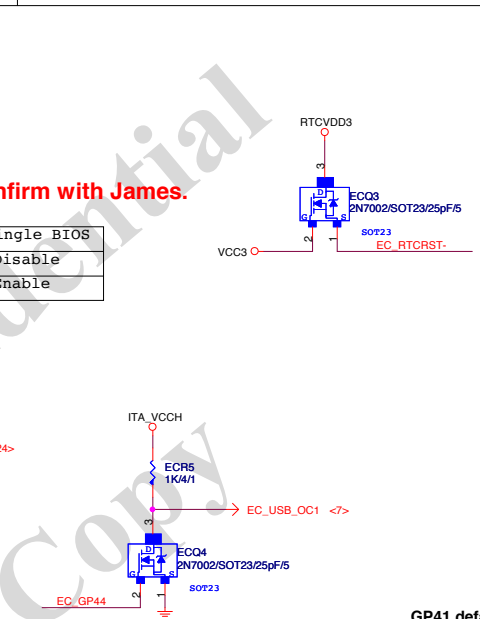
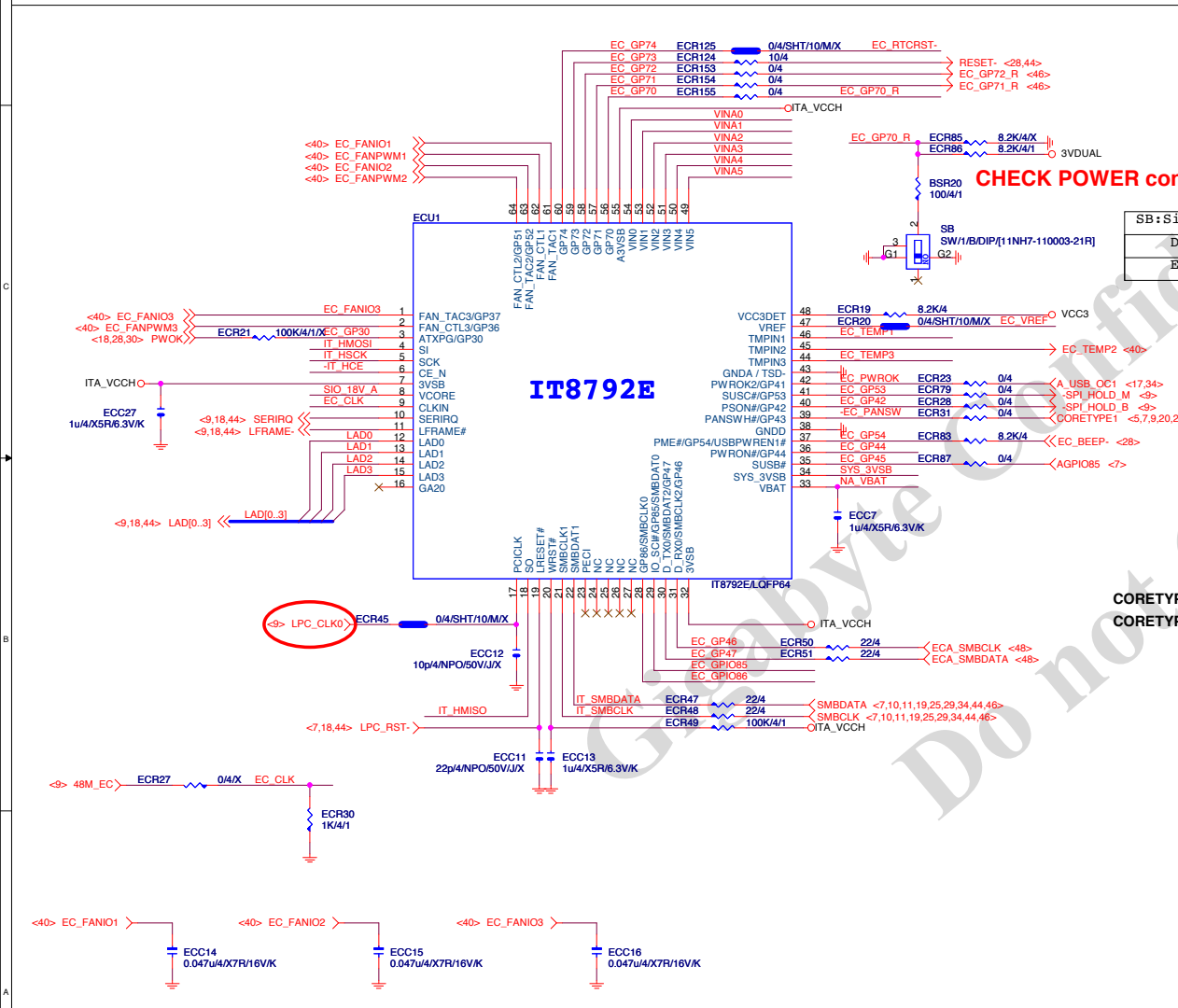
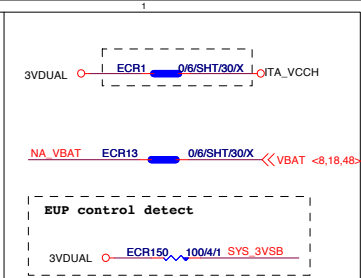
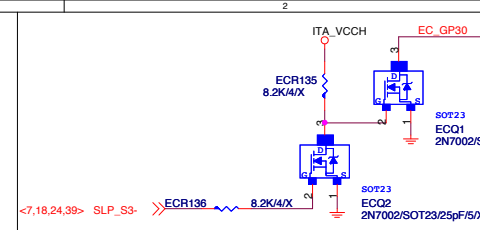
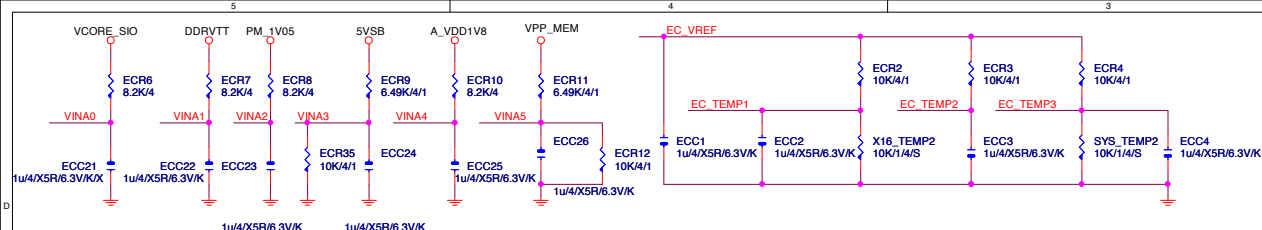
KBL FAN LOCATION MAP REFER TO PAGE.27

GIGABYTE

Title **PCIE X8, SWITCH**

Size Custom Document Number **GA-AX370-GAMING K7** Rev **1.0**

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To PCIe host.

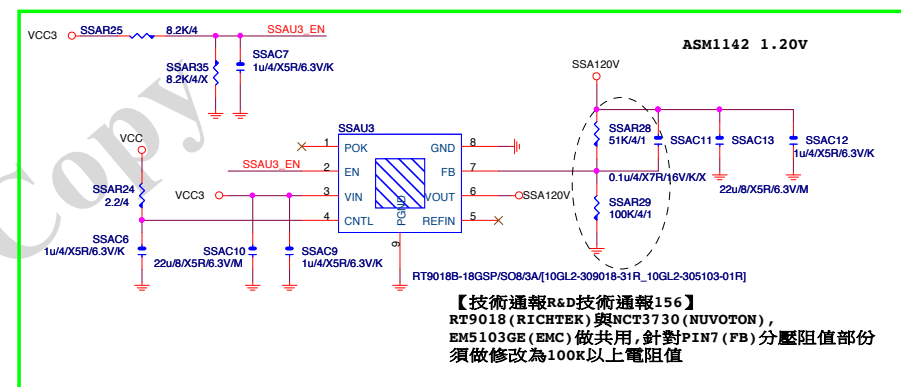
ASM1143 USB3.1

Base on ASM1142 0.3 Reference SCH

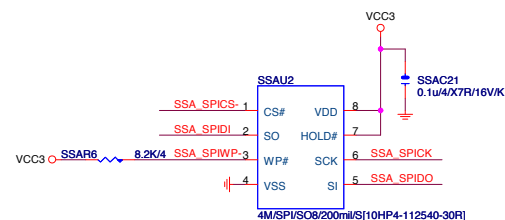


→ To OC circuit

To USB Contr

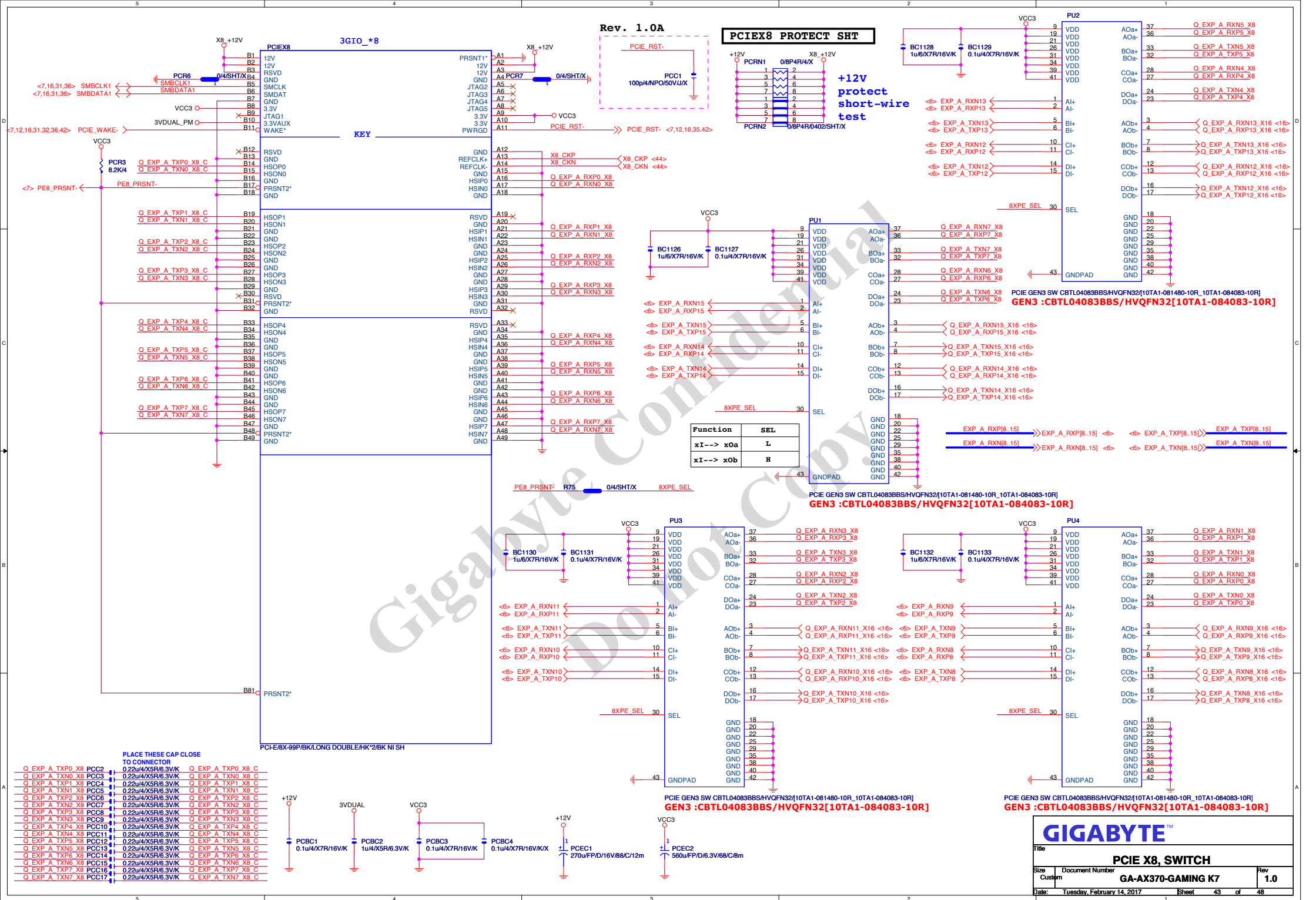


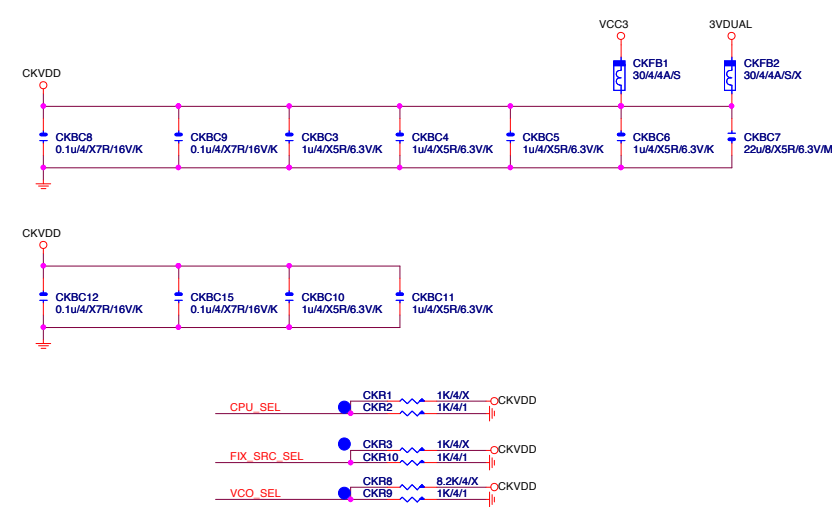
【技術通報R&D技術通報156】
RT9018 (RICHTER) 與 NCT3730 (NUVOTON),
EM5103GE (EMC) 做共用, 針對 PIN7 (FB) 分壓阻值部份
須做修改為 100K 以上電阻值



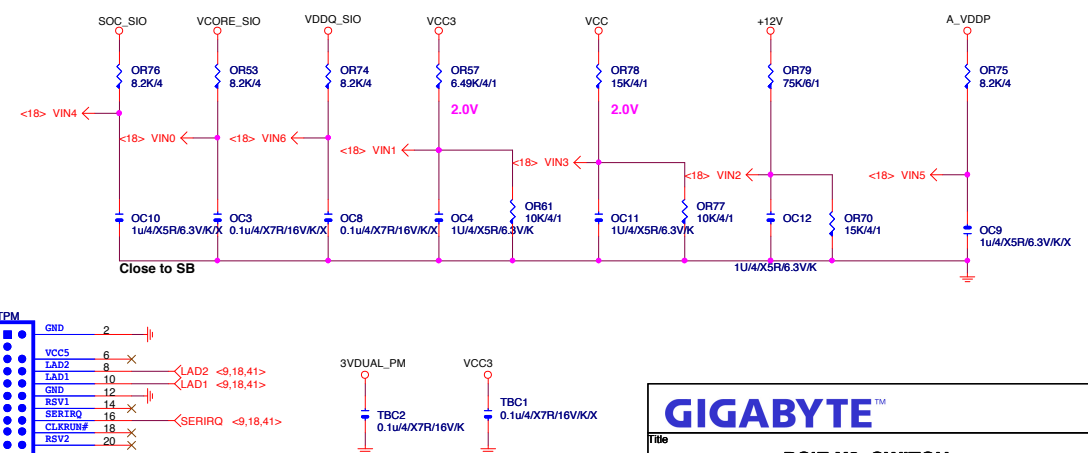
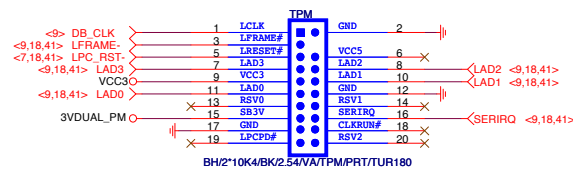
CSEL1	CSEL0	
1	1	External 20MHz Crystal (Asynchronous)
0	1	48MHz clock input (Synchronous)
X	0	Reserved for Test

				
Title				
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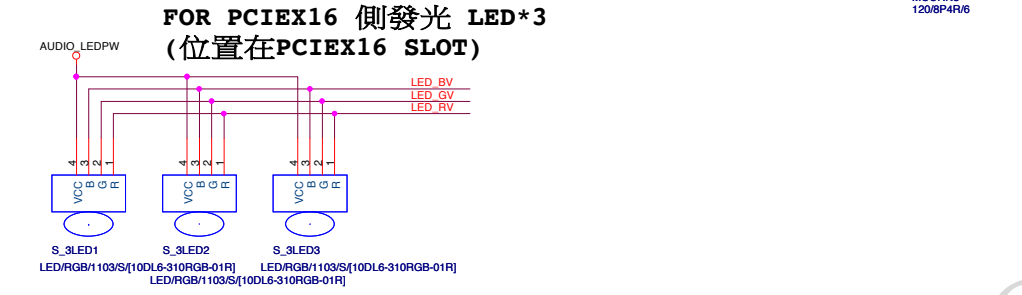
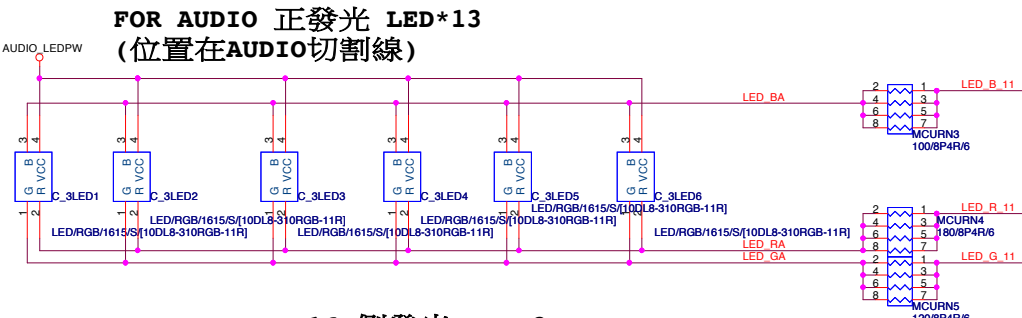


FSLB	FSLA	BCLK
1	1	100M
1	0	125M
0	1	166M
0	0	250M



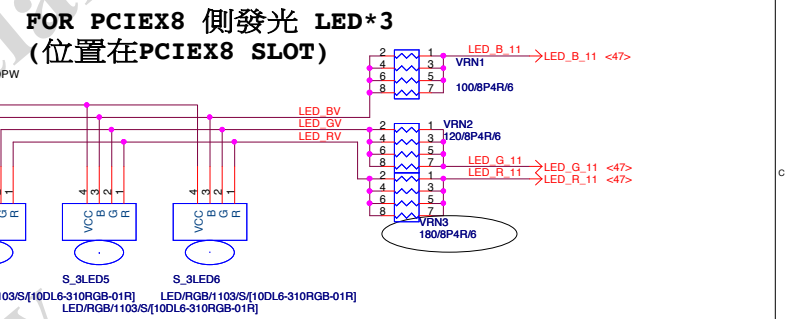
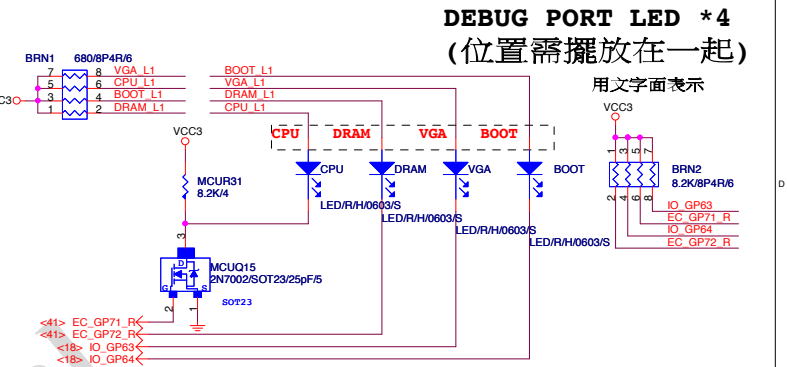
第一區 LED

Rev 0.63

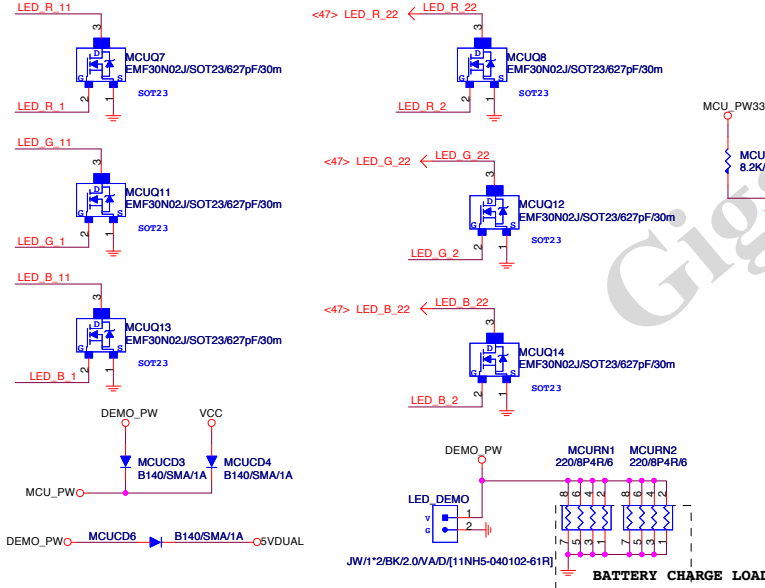


LED GPIO PIN DEFINE

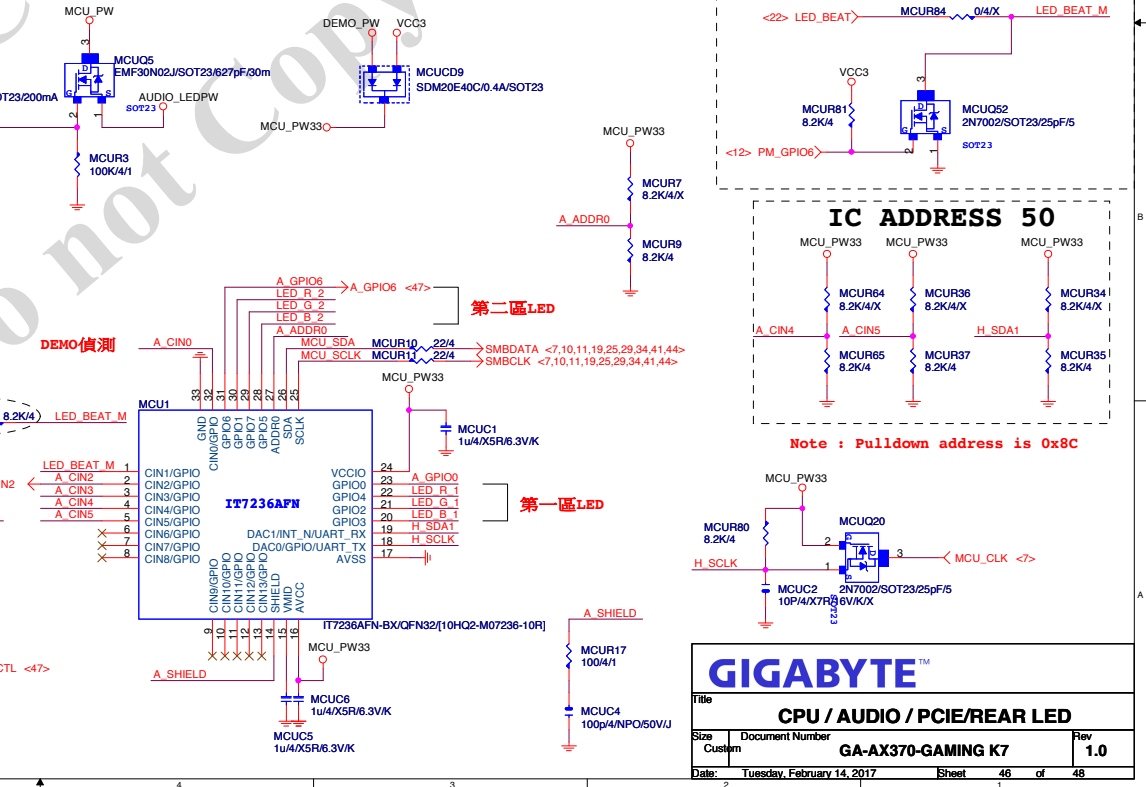
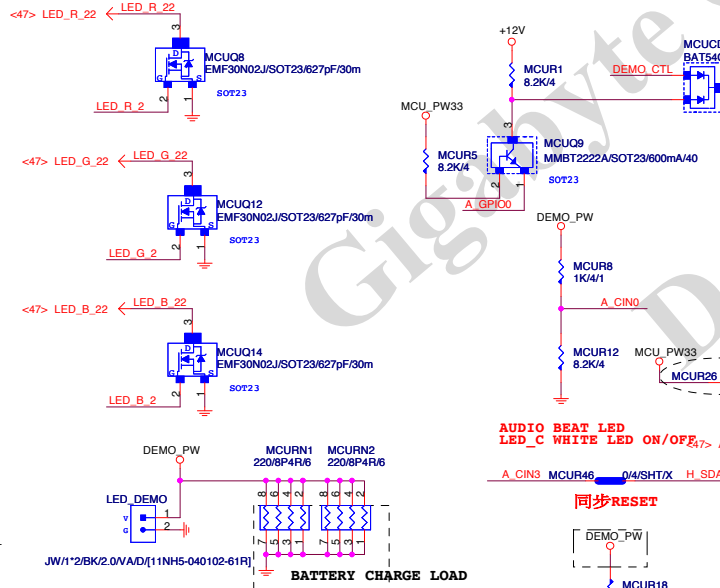
EC_GP71_R	CPU DEBUG
EC_GP72_R	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEBUG
PM_GPIO5	LED_C LED SWITCH
PM_GPIO6	PCIEX16 LED SWITCH
PM_GPIO7	PCIEX8 LED SWITCH



第一區 LED CONTROL



第二區 LED CONTROL



GIGABYTE

Title: CPU / AUDIO / PCIE/REAR LED

Size: Custom

Document Number: GA-AX370-GAMING K7

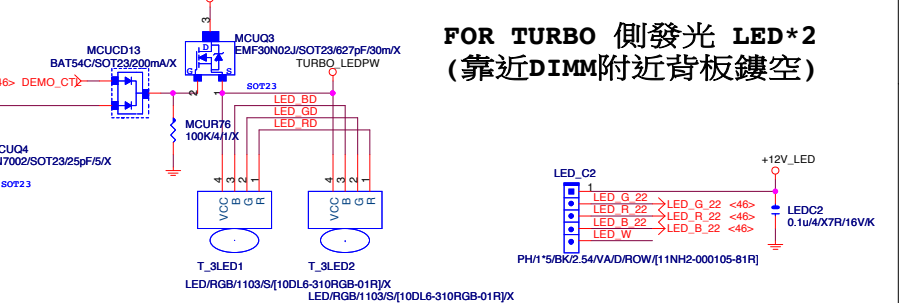
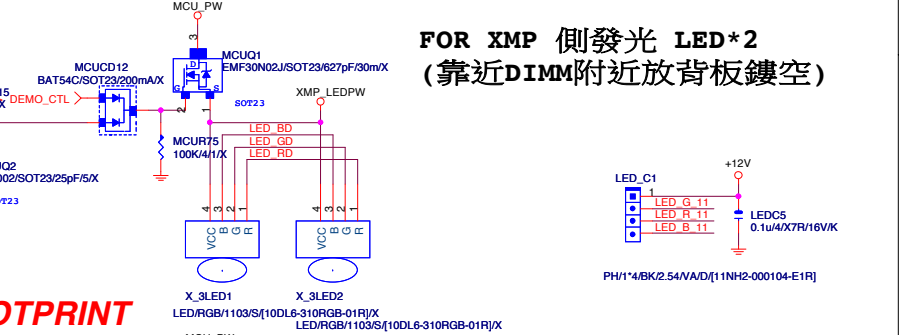
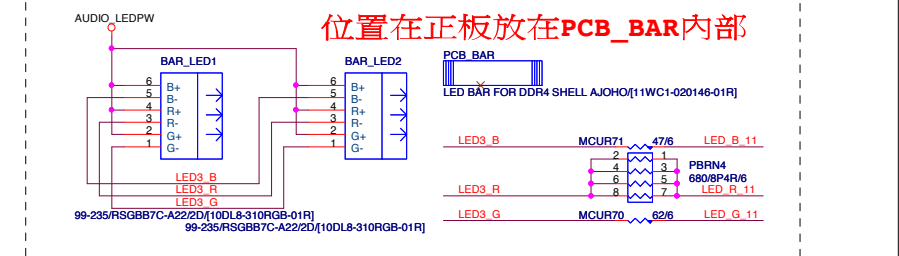
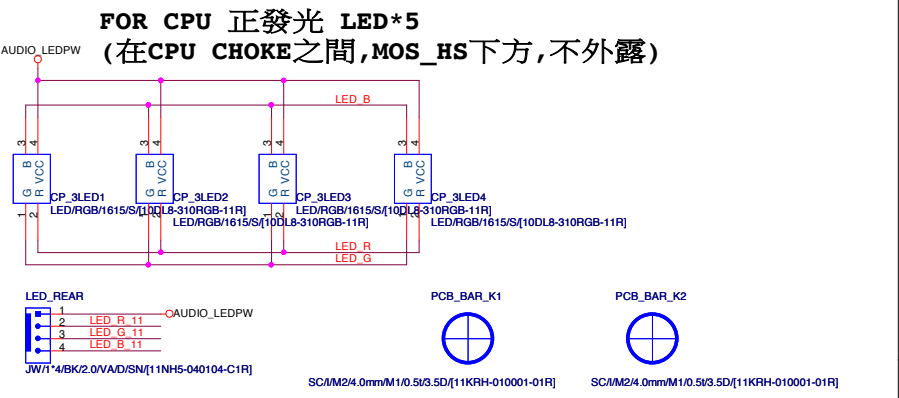
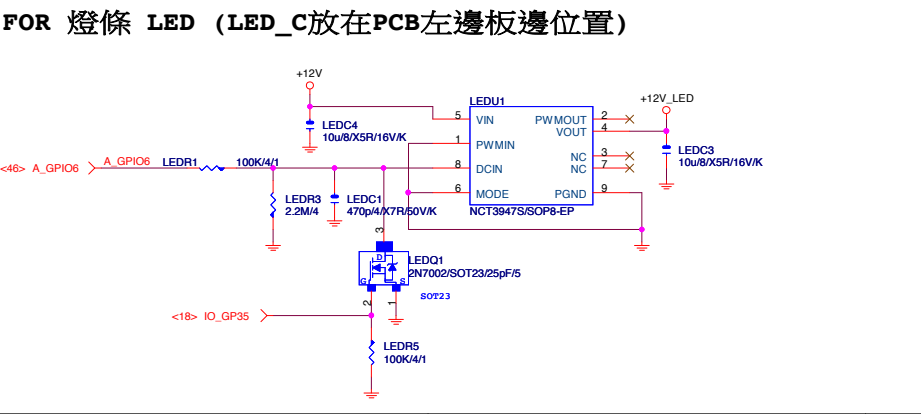
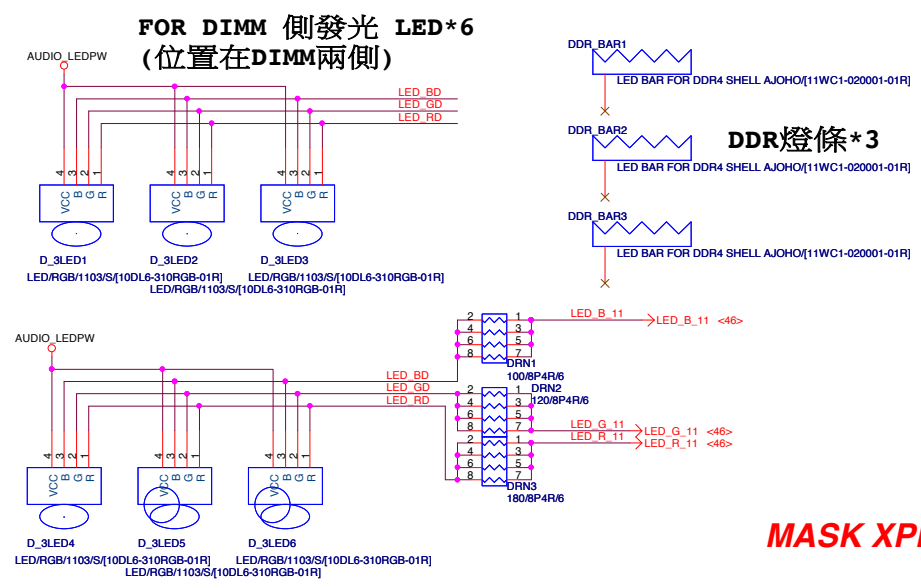
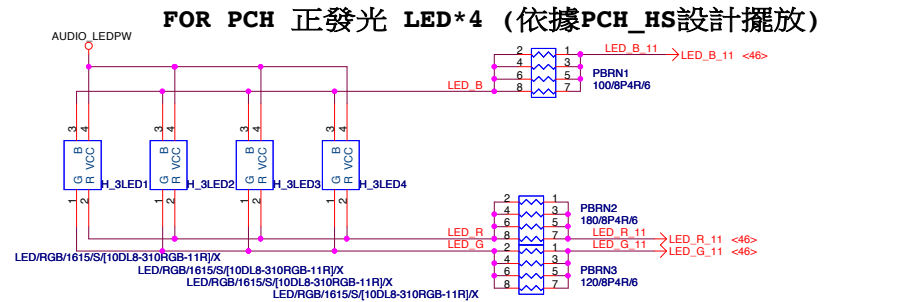
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第二區 LED

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MASK XPM AND TURBO??? FOOTPRINT

